June 23, 2004

VIA E-FILE

Hon. Edward M. Chen
United States Magistrate Judge
450 Golden Gate Ave.
San Francisco, CA 94102

Re: *Synopsys, Inc. v. Ricoh Company, Ltd.*
Case No. C03-02289 MJJ (EMC) and
Ricoh Company, Ltd. v. Aeroflex, Inc., et al.
Case No. C03-04669 MJJ (EMC)

Dear Magistrate Chen:

Pursuant to the Court's directives during the June 16 hearing and the Order of June 17, 2004, the parties have met and conferred with respect to Synopsys and the ASIC Defendants' invalidity contentions. As a result of these negotiations, Synopsys and the ASIC Defendants have agreed in principle to supplement some of their invalidity contentions by July 6, but they have refused to adopt Ricoh's proposed stipulation memorializing this agreement. There also are three areas on which the parties disagree about whether supplementation is necessary. This letter briefly sets forth Ricoh's understanding of the areas on which parties have agreed to supplement, and then discusses the areas of dispute. The positions of Synopsys and the ASIC Defendants follow.

Ricoh's Position

Chief Judge Patel recently emphasized that the Patent Local Rules "exist to further the goal of full, timely discovery and provide the parties with adequate notice and information with which to litigate their cases, not to create supposed loopholes through which parties may practice litigation by ambush." *Ixys Corp. v. Advanced Power Tech., Inc.*, No. C 02-03942 MHP, 2004 U.S. Dist. LEXIS 10934, June 16, 2004 (striking improper invalidity disclosures). Ricoh's objective is to ensure that Synopsys and the ASIC Defendants provide "full, timely discovery" and not attempt to ambush Ricoh by failing to properly disclose their positions.

Attached as Exhibit A is a proposed order that summarizes Ricoh's position. Paragraphs 1-5 of Exhibit A reflects the scope of the supplementation that Ricoh understands that Synopsys and the ASIC Defendants have committed to provide by July 6. The proposed language closely tracks the court's June 17 order with respect to Ricoh's infringement contentions. The proposed language covers the following points:

- Mapping (paragraph 1): Ricoh contends that Synopsys and the ASIC Defendants' invalidity contentions failed to specifically map or otherwise explain or relate the quoted prior art language to the disputed claim terms in the patent, creating

considerable ambiguity. Synopsys and the ASIC defendants have agreed to supplement to make clear how each quoted excerpt from the alleged prior art specifically relates to each claim element.

- Greater Specificity (paragraph 2): The invalidity contentions are replete with the same type of indefinite or qualifying language (such as "for example," "including", "may," "etc.") that Synopsys and the ASIC Defendants pilloried Ricoh. Applying the "goose and gander" rule, Synopsys and the ASIC Defendants have agreed to remove these indefinite terms and provide the same level of specificity as Ricoh has provided in its supplemental infringement contentions.

- Identification of prior art (paragraph 3): Synopsys and the ASIC Defendants have agreed to comply with Patent L.R. 3-3(a) by appropriately identifying prior art under 35 U.S.C. § 102(b) and/or (g).

- Identification of claims and bases for enablement (paragraph 4): Synopsys and the ASIC Defendants have agreed to comply with Patent L.R. 3-3(d).

- Synopsys and the ASIC Defendants have agreed to the production of all materials required by patent L.R. 3-2 (paragraph 5).

The proposed language closely tracks the Court's June 17 Order with respect to Ricoh's infringement contentions. Synopsys and the ASIC Defendants have not said why they object to this proposed language, other than stating that there is "no need" for such a stipulation or order. Ricoh believes that clearly articulating the parties' obligations is important. Ricoh submits that a stipulation or an Order is also appropriate because the meet and confer is the result of a Court Order, and is to resolve issues in lieu of a motion to compel.[1]

The parties are at an impasse with respect to three issues regarding the invalidity contentions:

1. Should Synopsys and the ASIC Defendants comply with Patent L.R. 3-3(b) and identify "each such combination" of prior art that they contend "makes a claim obvious," as well as the "motivation to combine" each such item.

Patent L.R. 3-3(b) states (emphasis added):

[1] Synopsys and the ASIC Defendants argue that Ricoh's June 21 supplementation failed to comply with the June 17 Order. Ricoh obviously disagrees with this assertion, and it believes that its supplementation addressed every aspect of the Order. Nevertheless, the question of whether Ricoh's supplementation is sufficient is not before the Court and does not control whether the invalidity contentions comply with the Patent Local Rules and this Court's instructions.

> Not later than 45 days after service upon it of the "Disclosure of Asserted Claims and Preliminary Infringement Contentions," each party opposing a claim of patent infringement, shall serve on all parties its "Preliminary Invalidity Contentions" which must contain the following information: . . . (b) Whether each item of prior art anticipates each asserted claim or renders it obvious. **If a combination of items of prior art makes a claim obvious, each such combination, and the motivation to combine such items, must be identified.**

The invalidity charts of Synopsys and the ASIC defendants (Ex. B and C) identify 17 different "prior art systems." Each of these "prior art systems" are in turn represented by a large number of individual documents. Synopsys and the ASIC Defendants have identified over 230 different items of prior art, comprising thousands of pages of documents, and they generally aver that Ricoh's '432 patent is invalid because these hundreds of items of prior art can be combined in ways to render each claim obvious. *But Synopsys and the ASIC Defendants have failed to identify a* ***single combination*** *of prior art that "makes a claim obvious."* Instead, they have amalgamated the hundreds of items of prior art into 17 "prior art systems," in violation of Patent L.R. 3-3(b)'s requirement that "for each item of prior art . . . each such combination, and the motivation to combine such items, must be identified."

Synopsys and the ASIC Defendants even have failed to identify specific combinations of the "prior art systems." Instead, they have provided lists of these prior art systems and generally asserted that any combination from List A and List B would make a claim obvious. See Ex. B at 8-10; Ex. C at 10-13. Ricoh should not be obligated to try to guess which combination of items of prior art, let alone which litigation-created amalgamation of prior art, could somehow be combined, or deduce any motivation for combining these widely varied references.

During the meet and confer, counsel for Synopsys and the ASIC defendants conceded that they were not going to go to trial with hundreds of items of prior art and 17 "prior art systems," but refused to narrow their identification of combinations of items of prior art to those that were really going to be at issue. Absent such an identification, the invalidity contentions is nothing more than a series of "loopholes through which parties may practice litigation by ambush," *Ixys Corp., supra,* slip op. at 7, that fails to comply with the rules and fails to put Ricoh and the Court on notice of the bases for the invalidity theories. After demanding exacting compliance of the Patent Local Rules by Ricoh, Synopsys and the ASIC Defendants should similarly be held to the same high standard and this Court already has indicated that they would be. They should identify, for "each item of prior art" (and not an imaginary "prior art system") "each such combination, and the motivation to combine such items."

2. Should Synopsys and the ASIC Defendants remove their alternative invalidity theories that are inconsistent with their proffered claim construction so the issues are appropriately narrowed for the Court? Synopsys and the ASIC defendants' invalidity charts contain three, four, even five alternative theories, only one of which is consistent with their proposed claim construction. Although they claim that the inclusion of such alternative theories

is to preserve their rights in case the Court adopts an alternative claim construction, they concede that Patent L.R. 3-6(b)(2) expressly permits such amendment without leave of Court. By including these alternative theories, Synopsys and the ASIC Defendants are cluttering rather than simplifying the issues. These alternative theories serve no useful purpose and should be stricken.[2]

3. Should Synopsys and the ASIC Defendants comply with Patent L.R. 3-3(d) and identify "any grounds of invalidity based upon indefiniteness under 35 U.S.C. § 112(2) or enablement or written description under 35 U.S.C. § 112(1) of any of the asserted claims"? Although Synopsys and the ASIC Defendants have already agreed to identify which of the claims they contend are invalid due to indefiniteness or lack of enablement, they refuse to disclose all facts supporting those contentions. Instead, they simply mimic the statutory language and then merely conclude that the claims are indefinite or insufficiently enabled. The rule requires the disclosure of "any grounds." Just as Ricoh was required to disclose all knowledge reasonably available to it as of the date of its supplemental infringement contentions, so should Synopsys or the ASIC Defendants be required to disclose all knowledge reasonably available to them as of July 6, 2004 – the date already identified by the Court for the service of the supplemental invalidity contentions. In their response, Synopsys and the ASIC Defendants argue that they need not disclose at this time facts already known to them that support these defenses, but may instead delay such disclosure until after the issuance of the Markman ruling. This argument is directly counter to the teaching of Chief Judge Patel in *Ixys Corp.*, as well as the Court's instruction at the June 16 hearing "you are going to put in everything you currently know." (6/16/04 Tr. at p. 5, lines 6-7.) Synopsys and the ASIC Defendants should be held to the same standard as Ricoh, and they should disclose "everything [they] currently know."

Paragraphs 8-10 of Ricoh's proposed order addresses these foregoing points.

Synopsys' insufficient responses to Ricoh's noninfringement interrogatory. There is one last issue pertaining to the claim construction briefing. Synopsys' amended declaratory judgment complaint alleges that none of its "Design Compiler Products" infringes either the '432 or '016 patent. Last year, Ricoh served interrogatories upon Synopsys seeking "each and every reason that tends to support or relates to" these allegations. (Ex. D, interrogatory nos. 2 and 3.) Instead of providing a fulsome statement of its noninfringement position, Synopsys instead provided nothing more than conclusory assertions that "the Synopsys Accused Software does not perform any step of" anything in the patent. (*Id.*) These responses were deficient when made, since Synopsys was obligated to disclose its claim construction position to support its noninfringement contentions. These interrogatory responses are even more deficient today, as

[2] Synopsys and the ASIC Defendants claim that the withdrawal of their alternative theories could mean that the charts "talk past each other." But Ricoh does not object here to invalidity theories that are either responsive to Ricoh's claim construction, or consistent with Synopsys and the ASIC Defendants' proposed claim construction; rather it is the third, fourth and fifth alternative theories that are disconnected from the claim constructions of any party that have no useful purpose.

Synopsys has disclosed its claim construction position, and should now specifically state the bases for its noninfringement contentions so Ricoh and the Court can be properly prepared. Ricoh has made repeated requests for Synopsys to supplement, and although Synopsys has vaguely promised that it will do so, it refuses to commit to a date or articulate the standards for any such supplementation.[3] Because Synopsys has placed its noninfringement of both patents at issue, Synopsys should be obligated to respond to these interrogatories in detail by no later than July 6, 2004. Paragraph 11 of Ricoh's proposed order addresses this point.

Synopsys and the ASIC Defendants' Position

Synopsys and the Defendants respond to Ricoh's overall characterization of the dispute between the parties and the specific areas of disagreement identified by Ricoh above.

The first section of Ricoh's letter asks the Court to issue an Order compelling Synopsys and the customer defendants to supplement their chart in a manner that they have *already* agreed to do. There simply is no need for the Court's intervention or such an order.

On June 21, 2004, pursuant to this Court's June 17, 2004 Order, Ricoh Company, Ltd. ("Ricoh"), served supplemental preliminary infringement contentions. Unfortunately, Ricoh has made only superficial efforts to comply with the Court's June 17 order, and Ricoh's preliminary infringement contentions remain non-compliant with the Federal Rules of Civil Procedure and this Court's Patent Local Rules. Ricoh's supplemented infringement charts continue to provide only the vaguest explanation as to how many of the elements in its claims relate to Synopsys' products. Furthermore, Ricoh is now in contempt of this Court's June 17, 2004 order requiring it to provide preliminary infringement contentions that do comply with the Patent Local Rules. Defendants will, if necessary, move this Court *again* to force Ricoh to fulfill its obligations and provide compliant preliminary infringement contentions.

Despite Ricoh's inadequate supplementation, and while Synopsys and the Defendants believe that their original preliminary invalidity contentions were in compliance with the Patent Local Rules, we have committed to supplement these charts to provide any additional explanation of how the passages cited in the preliminary invalidity charts relate to Ricoh's claims. That supplementation will reflect, and be responsive to, whatever explanation Ricoh has provided in its invalidity charts regarding how Synopsys' products relate to the asserted claims. Synopsys and the defendants will supplement their invalidity charts to demonstrate how any linkage made by Ricoh between its claims and Synopsys' products applies with equal or greater force to the prior art logic synthesis systems identified in the invalidity contentions.

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[3] In its response, Synopsys inconsistently claims that there has been no meet and confer on this issue, then acknowledges that there has been a meet and confer but incorrectly asserts that the issue was "tabled." Tellingly, Synopsys does not dispute that it promised to supplement these interrogatory responses. Thus, the only open issue is when that supplementation should be served, and the level of detail it should contain.

In addition, Synopsys and the customer defendants have committed to: (1) explicitly state that all of the asserted claims are subject to each of the Section 112 defenses identified in the initial preliminary invalidity disclosures, and (2) to explicitly state whether a 102(g) assertion is being made with reference to each prior art logic synthesis system.

Since the parties have reached an agreement on these matters (addressed in paragraphs 1-6 of Ricoh's proposed order), Synopsys and the Defendants believe that it is unnecessary to burden the Court and improper to seek an order imposing obligations already assumed.

Synopsys and the Defendants now turn to the three areas in which Ricoh asserts the parties disagree. Here, in each instance, Synopsys and the Defendants have complied with the Patent Local Rules. Ricoh simply has no basis for the relief to which it claims it is entitled.

1. Synopsys and the Defendants have complied with Patent L.R. 3-3(b).

Ricoh's allegations here are based on a false characterization of Synopsys and the Defendants' Preliminary Infringement Contentions. Contrary to what Ricoh asserts in its letter, the Preliminary Invalidity Contentions identify specific prior art systems and teachings that may be combined.

The Preliminary Invalidity Contentions separately discuss five different types of combinations that might be relevant under Section 103. Each of these combinations relates to a specific element of a logic synthesis system, that is missing from some other references cited in the Preliminary Invalidity Contentions. Those missing elements are:

- a graphical flowchart system for entering design data
- an expert system knowledge base used in carrying out logic synthesis
- the concept of synthesizing both data paths and control paths
- a capacity for simulating the input designs
- a capacity for generating mask data

These "missing elements" are high-level architectural features of a logic synthesis system. The Preliminary Invalidity Contentions treat each of these elements separately. The Contentions identify systems that do not have these elements, systems that do and specific reasons, many of which drawn from specific citations in the literature, as to why one of ordinary skill in the art would recognize that the particular feature at issue found in some of the prior art logic synthesis systems might be deployed in other prior art logic synthesis systems.

The Contentions, therefore, identify that each of the systems missing the particular element at issue might be combined with teachings of any one of the systems that includes that element. Ricoh's objection cannot be that it is unclear what references are being proposed for combination but, rather, that there is not particularized discussion of how one reference would be combined with another. In this case, however, the "missing elements" are purely architectural in nature. No specific implementation of "a graphical flowchart system" or "an expert system

knowledge base," is called for and there is, therefore, no reason to believe that the teachings of any of the logic synthesis systems including such properties are any more or less relevant than the teachings of any other.[4]

2. Synopsys and the Defendants presentation of alternative theories of invalidity are consistent with the Patent Local Rules and do not harm Ricoh.

Next, Ricoh's argument that Synopsys and the Defendants must limit their theory of invalidity at this stage is meritless.

First, there is nothing in the Local Patent Rules that prevents Synopsys and the Defendants from trying to anticipate different possible interpretations of the claims by the Court, and describe how their invalidity contentions would be altered based on these different interpretations and how the '432 patent would be invalid under these alternative claim constructions.

Furthermore, Ricoh is not harmed by the fact that the Preliminary Invalidity Contentions identify the invalidity arguments that might be made over the full range of possible claim constructions. If, as Ricoh proposes, the Preliminary Invalidity Contentions address only the prior art relevant to the claim constructions advanced by Synopsys and the customer defendants, the preliminary invalidity contentions and the preliminary infringement contentions will end up talking past each other, since each will be based on a separate claim construction.

3. Synopsys and the Defendants have complied with Patent L.R. 3-3(d).

Last, Ricoh's argument that Synopsys and the Defendants have failed to comply with Patent L.R. 3-3(d) is similarly meritless. In their preliminary invalidity contentions, Synopsys and the Defendants have in fact provided Ricoh with the precise claim language or system feature that renders each of the '432 patent claims indefinite and not enabled.

It appears that Ricoh is trying to create a dispute based on the definition of the term "grounds" in the Patent Local Rule. Ricoh would like the Patent Local Rule requirement for a description of the "grounds of invalidity" to be a requirement that Synopsys and the Defendants disclose all facts that they will ultimately rely on to establish how persons of ordinary skill in the art might interpret the patent and what they would be able to do with the Ricoh patent disclosure, or be precluded from proving those contentions later. However, that is not the purpose of the Patent Local Rules, nor the purpose of Patent L.R. 3-3(d). As Ricoh frequently points out, the Patent Local Rules are designed to "further the goal of full, timely, discovery and provide the

[4] If the Court examines the disclosure contained within the '432 patent, it will discover that there is little if any disclosure or discussion of the details of the architectural elements of the disclosed logic synthesis system or how those elements are connected together.

parties with adequate notice and information with which to litigate their cases." *Ixys Corp.*, 2004 U.S. Dist. LEXIS 10934, at *8.

Synopsys and the Defendants have provided Ricoh with the information required by Patent L.R. 3-3(d) to put Ricoh on notice of the grounds for invalidity on which they intend to rely. The preliminary invalidity contentions specifically identify which features of Ricoh's logic synthesis system are not adequately enabled. The detailed factual information required to support those contentions will be disclosed as it is developed, and in accordance with discovery plan to be formulated by the Court after claim construction.

4. Ricoh's request for an order to compel Synopsys' interrogatory responses is not properly before the Court.

The Court's June 17, 2004 order provides that: "If the parties, after a good faith meet and confer, are unable to reach agreement as to any dispute about the adequacy of Defendants' preliminary invalidity contentions, then the parties may file a short joint letter brief by June 23, 2004. Despite the fact that this issue is not relevant to the preliminary invalidity contentions and therefore, not properly addressed in this Joint Letter, Synopsys will attempt to address Ricoh's unfounded accusations.

First, Ricoh once again attempts to sandbag Synopsys by rejuvenating issues resolved in prior meet and confers. Specifically, in the last meet and confer between the parties regarding Synopsys' responses to Ricoh's Interrogatory Nos. 2 and 3 and Ricoh's response to Synopsys' Interrogatory No. 6 (relating to Ricoh's invalidity contentions regarding the Darringer et al. prior art), the parties agreed to table these issues. In other words, because of the Court's limitation on discovery to that which relates to claim construction, the parties agreed that they would only pursue responses to interrogatories on issues for which the other party had the burden of proof (i.e., Ricoh's infringement contentions and Synopsys' invalidity contentions). There has been no further meet and confer regarding any of these interrogatories since that agreement. Ricoh's attempt to renege on its agreement to table this issue should be rejected.

Second, these two interrogatory responses adequately set forth the reasons why Synopsys' Design Compiler Products do not infringe, which is an issue for which Ricoh has the burden of proof. Ricoh has not established that these responses are inadequate. And, contrary to Ricoh's assertions, these interrogatories do not require Synopsys to set forth a claim construction position. Besides this, Synopsys' preliminary claim constructions have already been provided to Ricoh pursuant to the local rules and its proposed constructions will be provided in the Joint Claim Construction Statement to be filed on July 13, 2004. Thus, this issue is not properly before this Court and there is certainly no basis for the relief Ricoh requests.

In conclusion, Ricoh's proposed order overreaches on every point by attempting to impose the Court's authority unnecessarily on issues where the parties have reached an agreement and by seeking relief on issues where no relief is justified.

Very truly yours,

Dated: June 23, 2004

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

SYNOPSYS, INC., Plaintiff, vs. RICOH COMPANY, LTD., Defendant.	**CASE NO. C-03-2289-MJJ (EMC)** **CASE NO. C-03-4669-MJJ (EMC)**
RICOH COMPANY, LTD., Plaintiff, vs. AEROFLEX INCORPORATED, et al., Defendants	**[PROPOSED] ORDER REGARDING DEFENDANTS' AND SYNOPSYS' PATENT L.R. 3-3 DISCLOSURES**

Based upon Ricoh's complaints regarding the invalidity disclosures of Defendants Aeroflex, Inc., AMI Semiconductor Inc., Matrox Electronic Systems, Ltd., Matrox Graphics Inc., Matrox International Corp., and Matrox Tech, Inc. (collectively "Defendants"), and Synopsys, Inc. ("Synopsys"), and in view of the Court's comments of May 27, 2004 and June 16, 2004, the Court's Order of June 17, and the Parties' June 23, 2004 letters to the Court, the Court hereby ORDERS as follows:

1. Defendants and Synopsys SHALL serve, via mail and email, on Ricoh, on or before July 6, 2004, an amended Patent L.R. 3-3 disclosure that, to the extent reasonably possible based upon information currently available to Defendants and Synopsys, unambiguously identifies where specifically in each alleged item of prior art each element of each asserted claim is found, including a description mapping and linking each alleged item of prior art to the claim language in each of the elements for each of the asserted claims. Such mapping and linking of the claim language to each

alleged item of prior art SHALL NOT include open ended language and SHALL be at the level of detail required by the applicable law and consistent with Magistrate Judge Chen's comments at the May 27, 2004 and June 16 hearings.

2. Defendants and Synopsys SHALL serve, via mail and email, on Ricoh, on or before July 6, 2004, an amended Patent L.R. 3-3 disclosure that, to the extent reasonably possible based upon information currently available to Defendants and Synopsys, responds in the same level of detail and specificity to Ricoh's June 21, 2004 amended Patent L.R. disclosure.

3. Defendants and Synopsys SHALL serve, via mail and email, on Ricoh, on or before July 6, 2004, an amended Patent L.R. 3-3 disclosure that, to the extent reasonably possible based upon information currently available to Defendants and Synopsys, complies with Patent L.R. 3-3(a) by identifying prior art under 35 U.S.C. § 102(b) by specifying the item offered for sale or publicly used and known, the date the offer or use took place or the information became known, and the identify of the person or entity which made the information known or to whom it was made known. Prior art under 35 U.S.C. § 102(g) shall be identified by providing the identities of the person or entities involved in and the circumstances surrounding the making of the invention before the patent application.

4. Defendants and Synopsys SHALL serve, via mail and email, on Ricoh, on or before July 6, 2004, an amended Patent L.R. 3-3 disclosure that, to the extent reasonably possible based upon information currently available to Defendants and Synopsys, complies with Patent L.R. 3-3(d) by identifying any grounds of invalidity based upon indefinitness under 35 U.S.C.§ 112(2) or enablement or written description under 35 U.S.C.§ 112(1) of any of the asserted claims, and specifically identifies each asserted claim for which these defenses are asserted.

5. Defendants and Synopsys SHALL serve, via mail and email, on Ricoh, on or before July 6, 2004, all materials required by Patent L.R. 3-4 and not previously produced.

6. This order and Defendants and Synopsys serving of an amended Patent L.R. 3-3 disclosure on July 6, 2004 shall not limit their rights under Patent L.R. 3-6 and 3-7 to further amend or supplement their amended Patent L.R. 3-3 disclosure.

7. The Parties acknowledge that this stipulation narrows but does not resolve all of the disputes they may have with respect to Defendants' and Synopsys' Patent L.R. 3-3 disclosures. The parties reserve all of their rights with respect to issues not addressed in this stipulation.

8. Defendants and Synopsys SHALL serve, via mail and email, on Ricoh, on or before July 6, 2004, an amended Patent L.R. 3-3 disclosure that, to the extent reasonably possible based upon information currently available to Defendants and Synopsys, complies with Patent L.R. 3-3(a) by identifying "whether each item of prior art anticipates each asserted claim or renders it obvious. If a combination of items of prior art makes a claim obvious, each such combination, and the motivation to combine such items, must be identified." Such identification of each item of prior art SHALL be done individually and SHALL NOT be consolidated into a "prior art system." When identifying a combination of items of prior art, each such combination, and the motivation to combine such items, SHALL be individually identified, and SHALL NOT be identified by grouping prior art into lists.

9. Defendants and Synopsys SHALL serve, via mail and email, on Ricoh, on or before July 6, 2004, an amended Patent L.R. 3-3 disclosure that, to the extent reasonably possible based upon information currently available to Defendants and Synopsys, is based upon their proposed claim construction, and SHALL NOT contain alternative positions not supported by any proposed claim construction.

10. Defendants and Synopsys SHALL serve, via mail and email, on Ricoh, on or before July 6, 2004, an amended Patent L.R. 3-3 disclosure that, to the extent reasonably possible based upon information currently available to Defendants and Synopsys, complies with Patent L.R. 3-3(d) and identifies "any grounds of invalidity based upon indefiniteness under 35 U.S.C. § 112(2) or enablement or written description under 35 U.S.C. § 112(1) of any of the asserted claims," and SHALL NOT be limited to conclusory and unsupported assertions.

11. Defendants and Synopsys SHALL serve, via mail and email, on Ricoh, on or before July 6, 2004, amended responses to Ricoh's noninfringement interrogatories (Ricoh's first interrogatories to Synopsys, nos. 2 and 3) that, to the extent reasonably possible based upon information currently available to Defendants and Synopsys, provides a fulsome statement of their noninfringement position, and SHALL NOT be limited to conclusory and unsupported assertions.

IT IS SO ORDERED:

Dated: _____

_____
HON. EDWARD M. CHEN

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD.,

Plaintiff,

vs.

AEROFLEX INCORPORATED, et al.,

Defendants.

SYNOPSYS, INC.,

Plaintiff,

vs.

RICOH COMPANY, LTD.,

Defendant.

Case No. C-03-4669 MJJ (EMC)
Case No. C-03-2289 MJJ (EMC)

PRELIMINARY INVALIDITY CONTENTIONS OF SYNOPSYS AND THE CUSTOMER DEFENDANTS PURSUANT TO PATENT L.R. 3-3 AND L.R. 3-4

Pursuant to Rule 3-3 of the Patent Local Rules of Practice in Civil Proceedings before the United States District Court for the Northern District of California ("Patent L.R."), Synopsys, Inc. ("Synopsys") and Defendants Aeroflex, Inc., AMI Semiconductor Inc., Matrox Electronic Systems, Ltd., Matrox Graphics Inc., Matrox International Corp., and Matrox Tech, Inc. (collectively "Defendants") submit the following Preliminary Invalidity Contentions ("Invalidity Contentions") in response to the Disclosure of Asserted Claims and Preliminary Infringement Contentions ("Infringement Contentions") submitted by plaintiff Ricoh Company, Ltd. ("Ricoh").

- Exhibits 1 through 19 provide Synopsys' and the Defendants' disclosure pursuant to Patent L.R. 3-3(c) for United States Patent No. 4,922,432 (the " '432 patent").
- The remainder of Synopsys' and the Defendants' disclosure pursuant to Patent L.R. 3-3(a), (b), (c), and their disclosure under subsection (d) for the '432 patent are contained herein.

Synopsys and Defendants base these Invalidity Contentions on their current knowledge, understanding, and belief as to the facts and information available as of the date of these contentions. Synopsys and Defendants have not yet completed their investigation, collection of information, discovery, or analysis relating to this action, and additional discovery may require them to supplement, amend and/or modify these contentions. More specifically, Ricoh has not produced all of the information responsive to Synopsys' discovery requests. Synopsys and the Defendants also have not had the opportunity to take any of the depositions of the named inventors of the '432 patent, and/or other persons having potentially relevant information. Synopsys and the Defendants also continue to search for additional invalidating prior art for the asserted claims of the '432 patent. Consequently, based upon a showing of good cause, Synopsys and the Defendants may subsequently seek an order from the Court allowing it to amend, modify, or supplement these contentions within a reasonable time after the discovery of any additional invalidating prior art.

Ricoh has also failed to comply with all of its disclosure requirements under Patent L.R. 3-1 and 3-2 and has also refused to provide information responsive to certain of Synopsys' Interrogatories. The specifics of these inadequacies are set forth in the Defendants' motion to strike

Ricoh's disclosures pursuant to Patent L.R. 3-1 and 3-2 and Synopsys' motion to compel responses to Interrogatory Nos. 1-3, respectively. Given these failures by Ricoh to comply with Patent L.R. 3-1, 3-2, and its discovery obligations, Synopsys' and the Defendants' position is that there is certainly good cause for subsequent amendment, modification, and/or supplementation of their Invalidity Contentions in the present actions based on information Ricoh is subsequently ordered to provide pursuant to either Synopsys' or the Defendants' motion. If and when Ricoh serves contentions that comply with all of the requirements of the applicable Patent Local Rules and proper responses to Synopsys' interrogatories, Synopsys and the Defendants will amend, modify, and/or supplement their Preliminary Invalidity Contentions, to the extent they deem necessary, within 45 days.

Synopsys' and the Defendants' ultimate contentions concerning the validity of the '432 patent claims may also change based upon the Court's construction of the claims and/or positions that Ricoh may take concerning claim construction, infringement, and/or validity issues.

The accompanying documents as well as the information provided below and in the Exhibits is provided for Synopsys' and the Defendants' compliance with Patent Local Rules 3-3 and 3-4 only. The information provided shall not be deemed an admission regarding the scope of any claims or the proper construction of those claims or any terms contained therein. The fact that documents have been identified below and produced with these Invalidity Contentions shall not be deemed an admission that such documents are admissible and/or that Synopsys and the Defendants have waived any objections regarding the admissibility of such documents.

DISCLOSURES UNDER PATENT L.R. 3-3(D)

I. INVALIDITY OF '432 PATENT UNDER 35 U.S.C. § 112

A. Knowledge Base Not Adequately Disclosed

The '432 patent fails to meet the "enablement" requirement of 35 U.S.C. § 112, because the '432 specification does not provide an explanation or disclosure of the expert system rules used by the described CAD system sufficient to allow one of ordinary skill in the art to build the expert system knowledge base referred to by the patent specification. The path synthesizer and cell selector (PSCS) software described in the specification relies on this knowledge base to perform a variety of

functions critical to successful operation of the system. *See, e.g.,* '432 patent, col.2 ll.58-63, col.4 ll.63-66, col.5 ll.6-8, col.5 ll.25-30, col.8 ll.21-30, col.8 l.65 – col.9 l.5, col.9 l.65 – col.10 l.12.

In particular, the '432 patent fails to provide sufficient information to allow one of ordinary skill in the art to implement an expert system knowledge base capable of performing: (1) selection of macros, (2) merging two macros, (3) mapping of macros to cells, (4) merging two cell, (5) error diagnostics. *See* '432 patent, col.8 l.65 – col.9 l.5. The '432 patent also fails to provide sufficient information to allow one of ordinary skill in the art to implement an expert system knowledge base capable of performing: (1) data path synthesis, (2) data path optimization, (3) macro definitions, (4) cell library, and (5) error detection and correction. *See* '432 patent, col.10 ll.1-7.

The failure to adequately describe the Knowledge Base may additionally constitute a violation of the written description and/or best mode requirements of 35 U.S.C. § 112. The applicants claimed to have a working copy of the KBSC software that is the subject of the '432 patent, but provided insufficient disclosure of the knowledge base. The operation of the Knowledge Base is implicated in at least the claim terms "expert system knowledge base," "knowledge base," "cell selection rules," "rules for selecting hardware cells," "data path rules," "generating control paths," "generating data paths," "cell selection means," "netlist generator means," "expert system means," "inference engine means," "generator means," the "selecting" step of claim 13, the "applying" steps of claims 18 and 19, and the "generating" steps of claims 15, 16, 17 and 20.

B. System Controller Generation Not Adequately Disclosed

The '432 patent fails to meet the "enablement" requirement of 35 U.S.C. § 112, because the '432 specification does not provide an explanation of how the described CAD system generates a system controller sufficient to allow one of ordinary skill in the art to build such a CAD system. The generation of a system controller is an essential element of the described CAD system. *See, e.g.,* '432 patent, col.1 ll.26-32, col.2 ll.40-42, col.4 ll.39-43, col.5 ll.9-13, col.6 ll.18-27, col.11 ll.49-51.

The failure to adequately describe the method used for system controller generation may additionally constitute a violation of the written description and/or best mode requirements of 35 U.S.C. § 112. The applicants claimed to have a working copy of the KBSC software that is the

subject of the '432 patent, but provided insufficient disclosure of the system controller generator. System controller generation is implicated in at least the claim terms "control generator means," and the steps of "generating control paths," and "generating a controller" found in claims 17 and 20.

C. Inference Engine Not Adequately Disclosed

The '432 patent fails to meet the "enablement" requirement of 35 U.S.C. § 112, because the '432 specification does not provide an explanation of the inference engine required by the described CAD system sufficient to allow one of ordinary skill to build such an engine. The '432 specification states that the rules interpreted by the engine must include: knowledge representation in the form of a record structure, conditional expressions in the antecedent of a rule, a facility to create and destroy structure in rule action and other capabilities. *See* '432 patent, col.10 ll.56-67. The patent specification does not provide any explanation of how to implement these required capabilities and the example rules provided do not provide any guidance since they are described in high level English rather than in the form that they would actually have to take in an operable system.

In addition, the '432 patent fails to describe how contexts are used during the operation of the PSCS software. The specification describes that contexts are required and that there can be context changes. *See* '432 patent, col.10 ll.13-37. The '432 specification, however, provides no information about how context changes are made and the relationship between contexts and the particular functions that the specification states are performed by the PSCS software. As a result, the patent specification does not provide sufficient information to enable one of ordinary skill in the art to build the system described in the specification.

The failure to adequately describe the design of the inference engine may additionally constitute a violation of the written description and/or best mode requirements of 35 U.S.C. § 112. The applicants claimed to have a working copy of the KBSC software that is the subject of the '432 patent, but provided insufficient disclosure of the inference engine. The inference engine is implicated in at least the claim terms "cell selection means," "netlist generator means," "expert system means," "inference engine means," "generating control paths," "generating data paths," the

"selecting" step of claim 13, the "applying" steps of claims 18 and 19, and the "generating" steps of claims 15, 17 and 20.

D. Timing Analysis Not Adequately Disclosed

The '432 patent fails to meet the "enablement" requirement of 35 U.S.C. § 112, because the '432 specification does not provide an explanation of how the described CAD system performs timing analysis of the target design. The '432 specification states that time delay is an important consideration in doing cell selection. *See* '432 patent, col.8 ll.26-30, col.8 ll.58-64, col.9 ll.52-61. The '432 specification, however, provides no information as to how the timing constraints on a design are to be established, how the timing performance of a design is calculated and how timing delay is then used in cell selection. Without this information it would be impossible for one of ordinary skill in the art to implement the system described in the specification.

The failure to adequately describe the design of the inference engine may additionally constitute a violation of the best mode requirements of 35 U.S.C. § 112. The applicants claimed to have a working copy of the KBSC software that is the subject of the '432 patent, but provided insufficient disclosure of any timing analysis element of that software.

E. "Architecture Independent" Lacks Adequate Definition

The '432 patent fails to meet the "written description" requirement of 35 U.S.C. § 112. The phrase "architecture independent" is used in the patent specification to distinguish the claimed invention from prior art logic synthesis systems. In the file wrapper for the '432 patent the claims of the '432 patent were distinguished from systems that perform logic synthesis on register transfer level specifications – and the 4,703,435 patent to Darringer et al. in particular – on the basis of the "architecture independent" phrase in the '432 patent claims. The phrase "architecture independent" is capable of a range of meanings, some of which would include register-transfer level descriptions and the descriptions used in the Darringer patent. Neither the text of the '432 patent nor the file wrapper, provide any explanation of what meaning this phrase is to have in the context of the '432 patent and claims. The term "architecture independent" appears in each independent claim, and its use invalidates each of the claims of the patent.

In addition, the phrase "architecture independent" introduces new matter to the patent specification, which is prohibited by 35 U.S.C. § 132.

DISCLOSURES UNDER PATENT L.R. 3-3(a) & 3-3(b)

II. INVALIDITY OF '432 PATENT UNDER 35 U.S.C. § 102(G)

Properly construed, the claims of the '432 patent do not read on Synopsys' Design Compiler or related products. If essential limitations of the '432 patent claims are ignored, broadening the claims so as to encompass the activities of Synopsys' Design Compiler, then individuals working at General Electric and/or other research institutions, including U.C. Berkeley, who formed Optimal Solutions and then Synopsys have a superior claim to inventorship than the named inventors of the '432 patent. The individuals who conceived of and developed the architecture of early GE / Optimal Solutions / Synopsys products included: David Gregory, Aart de Geus, William Cohen, Karen Bartlett, Karl Garrison, Gary Hachtel, Tim Moore, Russell Segal, Rick Rudell, Van Morgen and William Krieger. While each of these people may be a contributor to such an invention, the actual inventors would be determined by the scope of each claim as the Court construes it. The original conception of the architecture for GE / Optimal Solutions / Synopsys products dates back to at least 1984 and 1985. The exact date of conception and identity of the individuals forming this conception will depend upon how broadly the elements from the claims of the '432 patent are understood. Furthermore, Synopsys is not claiming that the individuals identified above are the original inventors of any general architecture relevant to this case, only that these individuals have a superior claim to inventorship of such an architecture than the persons named on the '432 patent.

Charts describing the application of ancestral versions of Design Compiler to the claims of Ricoh's patent are attached to this submission. These charts describe how the earliest version of the Design Compiler product operated and do not describe the operation of current or recent versions of Design Compiler, almost twenty years later.

III. INVALIDITY OF '432 PATENT UNDER 35 U.S.C. § 102(a) & (b)

The relevance of various prior art systems will depend upon the construction of the claims. The discussion below accounts for some, but not all, possible alternative claim constructions.

A. "a series of architecture independent actions and conditions" / "a flowchart comprised of elements representing a series of architecture independent actions and conditions"

If claim 13) is interpreted to require the use of a flowchart input constructed from a sequence of nodes describing functions to be performed or conditions to be tested, then the claims of the '432 patent are anticipated under 102(a) and (b) by the following prior art synthesis systems:

- MEGA
- IBM EDS
- CMU DAA

If the "input specification means" of claim 1, "flowchart editor means" of claims 4, 9 and 11, or the "describing" step of claims 13 and 18 are interpreted broadly enough to encompass systems that use Verilog and VHDL descriptions of the target design as design inputs, then the claims of the '432 patent are anticipated by each of the references listed above, as well as:

- SOCRATES
- Berkeley SYNTHESIS SYSTEM
- AT&T DAA
- HAL
- DAGON
- Fujitsu
- CATHEDRAL
- Carleton ELF
- FLAMEL
- CADDY
- CHIPPE
- NTT VLSI-DE
- PLEX
- MIMOLA & V-SYNTH

Charts describing the application of these prior art systems to the claims of Ricoh's patent are attached to this submission.

B. "expert system knowledge base / "knowledge base" / "inference engine"

If "expert system knowledge base" and "knowledge base" are properly construed to refer to a knowledge base used in an artificial intelligence expert system containing rules for use with an inference engine, the claims of the '432 patent are anticipated under 102(a) or (b) by a number of references, including:

- IBM EDS
- CMU DAA
- AT&T DAA
- HAL

- Fujitsu
- CATHEDRAL
- CHIPPE
- NTT VLSI-DE

If "expert system knowledge base" and "knowledge base" are not restricted to the meaning given to knowledge base in the field of artificial intelligence, and are interpreted to encompass any software tool that embodies heuristics or algorithms for logic synthesis, the claims of the '432 patent are anticipated by all of the references given above, plus:

- MEGA
- SOCRATES
- Berkeley SYNTHESIS SYSTEM
- Carleton ELF
- DAGON
- FLAMEL
- CADDY
- PLEX
- MIMOLA & V-SYNTH

C. "describing for a proposed application specific integrated circuit ..." / "specifying for each described action and condition ..."

If these claim elements are construed to refer to the process of selecting a series of generic actions and generic conditions followed by the process of identifying the specific action or specific condition intended for each of the generics by selecting an action or condition from a set of possible actions and conditions, the claims of the '432 patent are anticipated under 102(a) or (b) by the following prior art synthesis systems:

- MEGA
- IBM EDS

If these claim elements are construed to refer to any process in which a functional description of a target design is provided as input to a synthesis system, the claims of the '432 patent are anticipated by all of the references given above, plus:

- SOCRATES
- Berkeley SYNTHESIS SYSTEM
- CMU DAA
- AT&T DAA
- HAL
- DAGON

- Fujitsu
- CATHEDRAL
- Carleton ELF
- FLAMEL
- CADDY
- CHIPPE
- NTT VLSI-DE
- PLEX
- MIMOLA & V-SYNTH

D. "storing a set of definitions of architecture independent actions and conditions" / "a macro library defining a set of architecture independent actions comprised of actions and conditions" / "storing in a macro library a set of macros defining architecture independent actions and conditions"

One of these phrases appears in claim elements in each of claims 1, 9, 13 and 18. This language is believed to be inapplicable to synthesis systems that parse design inputs having a syntax defined by a language specification. Since Ricoh presumably disputes this, for the purposes of these preliminary invalidity contentions we have assumed a sufficiently broad construction that these claim terms would reach those synthesis systems.

E. Public Use or Sale

The following logic synthesis systems are believed to have been in public use more than one year prior to January 13, 1988:

i) IBM EDS

On information and belief, the IBM EDS system was publicly demonstrated at the 20th Design Automation Conference in Miami Beach, Florida in June of 1983, and shown to numerous potential customers that may have hired IBM to produce designs for their ASICs. The system had been used to make over 90 chip designs by 1984. Synopsys and Defendants will proceed with discovery to confirm these and other public uses and sales.

ii) MEGA

On information and belief MEGA was a public project at the University of Karlsruhle. A paper describing this system was published in the Proceedings of the IEEE Int'l Conf. On Computer Aided Design, which was held in Santa Clara, California in November of 1985. Additionally, there was a presentation of the MEGA system related to this published paper at the same conference. Synopsys and Defendants will proceed with discovery to confirm these and other public uses and sales.

iii) PLEX

PLEX was a project at AT&T Bell Labs. This system was published in the Proceedings of the 1983 Int'l Conference on Computer Aided Design in Santa Clara, California. On information and belief, there were presentations of the PLEX system related to these published papers the 1983 International Conference on Computer Aided Design. PLEX was demonstrated and presented to a number of interested individuals and/or companies, including at least Coleco and National Semiconductor, during tours of AT&T Bell Labs prior to the critical date of January 13, 1987. One such presentation was videotaped and broadcast on television. Such presentations generally included live demonstrations of the working system or screen shots of the working system. Synopsys and Defendants will proceed with discovery to confirm these and other public uses and sales.

iv) SOCRATES

On information and belief SOCRATES was demonstrated publicly at the Design Automation Conference in Las Vegas, Nevada in 1986. Beginning as a GE research project, SOCRATES papers were published and the system shown to potential customers including CALMA and others prior to the critical date. GE offered to sell SOCATES to Optimal Solutions by at least December of 1986 and sold the software to the new company at its inception, prior to January 13, 1987. Development of SOCRATES also occurred at public projects at Duke University and the University of Colorado. Synopsys and Defendants will proceed with discovery to confirm these and other public uses and sales.

v) Berkeley Synthesis System

This is a public project at The University of California at Berkeley. Students and professors used the system and published papers and theses regarding the system. On information and belief the source code for the system was available to public via ftp download prior to the critical date of January 13, 1987 for anyone's use. Individuals from GE, Optimal Solutions used this code in developing aspects of Synopsys' early products.

vi) DAA – CMU

CMU DAA was a public project at Carnegie Mellon University and sponsored by number of companies. The CMU DAA system was delivered to its sponsors by at least 1987. Students and professors used the system and published papers and theses regarding the system. This system was published in the Proceedings of numerous conferences and symposiums held in the United States

including: 20th Design Automation Conference held in Miami Beach, Florida, in June 1983; 22nd Design Automation Conference in Las Vegas, NV in 1985; and the 1983 Int'l Symposium on Circuits and Systems in Newport Beach, California, in May 1983. On information and belief, there were presentations of the CMU DAA system related to these published papers at their respective conferences. CMU DAA was publicly demonstrated and presented to a number of interested companies prior to the critical date of January 13, 1987. Such presentations included screen shots of the working system. Public benchmarks for comparing automatic logic synthesis systems were also run through the CMU DAA system and the results disseminated. Synopsys and Defendants will proceed with discovery to confirm these and other public uses and sales.

vii) DAA – ATT

AT&T DAA was a public project at AT&T. There were several published papers regarding the system. This system was published in the Proceedings of numerous conferences and symposiums held in the United States including: 23rd Design Automation Conference in Las Vegas, NV in 1986; and the 1986 Int'l Conference on Computer Design in Port Chester, NY in October, 1986. On information and belief, there were presentations of the AT&T DAA system related to these published papers at their respective conferences. AT&T DAA was publicly demonstrated and presented to a number of interested companies prior to the critical date of January 13, 1987. Such presentations included screen shots of the working system. Public benchmarks for comparing automatic logic synthesis systems were also run through the AT&T DAA system and the results disseminated. Synopsys and Defendants will proceed with discovery to confirm these and other public uses and sales.

viii) Fujitsu DDL/SX

Fujitsu DDL/SX was developed at Fujitsu Ltd. in Kawasaki, Japan and implemented LISP and C-Prolog. This system was published in the Proceedings of numerous conferences and symposiums including: IFIP Sixth International Symposium on Computer Hardware Description Languages and their Applications in Pittsburg, Pennsylvania in May 1983; Proceedings of the Fall Joint Computer Conference 1986, p.979-986, in November 1986 in Dallas, Texas; the 16th Design Automation Conference held in San Diego, California in June of 1979; 18th Design Automation Conference held in Nashville, Tennessee in June 1981; the 19th Design Automation Conference held in Las Vegas, Nevada in June 1982; 23rd Design Automation Conference held in Las Vegas, Nevada in 1986; and The International Conference On Computer Aided Design in Santa Clara, California in 1985.

Synopsys and Defendants will seek discovery of additional information regarding other public use, demonstration, or sale of the system.

ix) CHIPPE

Chippe was initially developed at the University of Illinois and later at Penn State and the University of California at Santa Barbara, the work was supported through funding from Gould Foundation and AT&T Bell Laboratories. Students and professors used the system and published papers regarding the system. This system was published in the Proceedings of the 23rd Design Automation Conference held in Las Vegas, NV in June of 1986, and the 24th Design Automation Conference held in Miami Beach, Florida in June of 1987. On information and belief Chippe was demonstrated and presented to AT&T prior to the critical date of January 13, 1987. Synopsys and Defendants will seek discovery of additional information regarding other public use, demonstration, or sale of the system.

x) HAL

HAL was developed at Carlton University with funding from BNR and The Natural Sciences and Engineering Research Counsel of Canada. This system was published in the Proceedings of the IEEE Int'l Conf. On Computer Design, which was held in Port Chester, New York in October of 1984 and the 23rd Design Automation Conference held in Las Vegas, Nevada in June of 1986. Synopsys and Defendants will seek discovery of additional information regarding other public use, demonstration, or sale of the system.

xi) NTT VLSI-DE

The NTT VLSI-DE system was developed at NTT in Tokyo, Japan, and implemented in LISP. This system was published in multiple proceedings including the IEEE Int'l Conf. On Computer Design, which was held in Port Chester, New York in October of 1984. Synopsys and Defendants will seek discovery of additional information regarding other public use, demonstration, or sale of the system.

xii) DAGON

DAGON was developed at AT&T with influence, and is possibly derives, from SOCRATES and the Berkeley Synthesis Project. The system was published in the Int'l Conference on Computer-Aided Design, which was held in Santa Clara, California, in November 9-12, 1986, and the 24th

Design Automation Conference held in Miami Beach, Florida in June of 1987. On information and belief, DAGON presented to interested companies prior to the critical date of January 13, 1987. Synopsys and Defendants will seek discovery of additional information regarding other public use, demonstration, or sale of the system.

xiii) FLAMEL

FLAMEL was developed and used at Stanford University under a DARPA contract. Students and professors used the system and freely published articles and dissertations regarding the unclassified project by at least the Summer of 1985. Synopsys and Defendants will seek discovery of additional information regarding other public use, demonstration, or sale of the system.

xiv) CATHEDRAL

Cathedral was jointly developed at the University of California at Berkeley, Phillips Research Lab, Interuniversity Micro Electronics Center, and Katholieke University, the work was sponsored by the EC under ESPRIT 97 contract. Students and professors used the system and published papers regarding the system. This system was published in the Proceedings of the IEEE Int'l Symposium On Circuits and Systems, which was held in San Jose, California in May of 1986 and the Int'l Conference on Computer-Aided Design, which was held in Santa Clara, California, in November 9-12, 1987. Synopsys and Defendants will seek discovery of additional information regarding other public use, demonstration, or sale of the system.

xv) CADDY

CADDY was developed at University of Karlsruhe with funding from Seimens and the DMFT of Germany. This system was published in multiple proceedings including the IEEE Int'l Conf. On Computer Design, which was held in Port Chester, New York in October of 1984, and the 22nd and 23rd Design Automation Conferences held in Las Vegas, Nevada in 1985 and 1986. There were presentations of the CADDY system related to these published papers at their respective conferences. Additionally, there were presentations of the CADDY system to U.S. corporations including, at least, IBM in 1984 and 1986. Synopsys and Defendants will seek discovery of additional information regarding other public use, demonstration, or sale of the system.

xvi) Carelton ELF

ELF was developed at Carlton University with funding from Northern Telecom Electronic and the Natural Sciences and Engineering Research Counsel of Canada. This system was published in the Proceedings of the IEEE Int'l Conf. On Computer Design, which was held in Port Chester, New York in October of 1984, and IEEE Int'l Symposium On Circuits and Systems, which was held in Philadelphia, Pennsylvania in May of 1987. Synopsys and Defendants will seek discovery of additional information regarding other public use, demonstration, or sale of the system.

xvii) MIMOLA/ VSYNTH

MIMOLA/VSYNTH was developed at Honeywell Inc., in Bloomington, MN and the University of Kiel. Professors and students, and Honeywell used the system and published papers, thesis and manuals regarding the system. This system was published in multiple proceedings including: the 16th Design Automation Conference held in San Diego, California in June of 1979; the 21st Design Automation Conference held in Albuquerque, New Mexico in June 1984; 23rd Design Automation Conference held in Las Vegas, Nevada in 1986; the 17th Annual Microprogramming Workshop, held in October and November of 1984 in New Orleans, LA, and the Proceedings of the 20th Annual Workshop on Microprogramming held in Colorado Springs, Colorado in December of 1987. Synopsys and Defendants will seek discovery of additional information regarding other public use, demonstration, or sale of the system.

DISCLOSURES UNDER PATENT L.R. 3-3(b)

IV. INVALIDITY OF '432 PATENT UNDER 35 U.S.C. § 103

A. Combination with References Teaching Flowchart Inputs

Each of the following claim elements implicates the use of a graphical flowchart system as a vehicle for providing input to a synthesis system:

- "input specification means" (col.14 ll.39-46)
- "specification means"[1] (col.14 l. 67 – col.15 l.2)
- "flowchart editor means" (col.15 ll.8-10)
- "flowchart editor means" (col.15 ll.39-41)
- "macro specification means" (col.15 ll.42-45)

[1] Per certificate of correction.

- "flowchart editor means" (col.16 ll.9-17)
- "describing for a proposed application specific integrated circuit ..." (col.16 ll.45-47)
- "specifying for each described action and condition ..." (col.16 ll.48-51)
- "describing for a proposed application specific integrated circuit a flowchart ..." (col.17 l.23 – col.18 l.2)
- "specifying for each described action or condition of said series ..." (col.18 ll.3-5)

The use of a graphical flowchart system as a method for providing input to a synthesis system is taught in the following references:

A-i. MEGA references
A-ii. IBM EDS references
A-iii. [Darringer85]
A-iv. [Michener71]
A-v. [Orailoglu86]
A-vi. [Director81]
A-vii. [Gustafson82]
A-viii. [Case81]

The teachings in these references to use a graphical flowchart system as a method for providing input to a synthesis system could be combined with the synthesis systems described in the following references to render the claims obvious:

A-1. SOCRATES
A-2. Berkeley SYNTHESIS SYSTEM
A-3. Ancestral DC
A-4. CMU DAA
A-5. AT&T DAA
A-6. HAL
A-7. DAGON
A-8. Fujitsu
A-9. CATHEDRAL
A-10. Carleton ELF
A-11. FLAMEL
A-12. CADDY
A-13. CHIPPE
A-14. NTT VLSI-DE
A-15. PLEX
A-16. MIMOLA & V-SYNTH

The motivation to combine these references can be drawn from several sources:

- The extensive cross-citation between articles describing these systems.

- The fact that the literature describing synthesis systems generally recognized that inputs to synthesis systems could take a variety of different forms, including flow graphs and flow charts. See Ex. 19, section 2, infra.

- The fact that the literature describing synthesis systems described that they were built as hierarchies of modules and that data produced as output from one module could be supplied as an input to another module within the synthesis system. See Ex. 19, section 7. The outputs of the flowchart input modules of references could, with appropriate modification, be integrated with existing modules of systems A-1 through A-15.

- The [Darringer85] article (A-iii) advocated the use of flowcharts as design inputs for logic synthesis systems. [Darringer85] at xv, xix.

- The [Michener71] article (A-iv) advocated the use of flowcharts as a means of describing a system design. [Michener71] at 42.

- The [Orailoglu86] article (A-v) advocated the use of flow graphs as a design input to silicon compilers, and proposed that behavioral descriptions could be converted to flow graph representations, which would then be provided as input to the silicon compiler. [Orailoglu86] at 506-509.

- The [Director81] article that bluntly acknowledges that it is simply a design choice to provide input through a graphical flowchart or through textual input. [Director81] at 635.

- The [Case81] reference points out the flowchart description for synthesis is a graphic form of a RTL description, and identifies the algorithm for the flowchart translator as previously published information. [Case81] at 637, 2nd col. *See also* [Gustafson82] at 18, 2nd col. and 20, 2nd col.

B. Combination with References Teaching Use of An Expert System Knowledge Base

Each of the following claim elements implicates the use of an expert system knowledge base:

- "said cell selection means comprising an expert system including a knowledge base containing rules …" (col.14 ll.50-59)
- "a knowledge base containing rules for selecting data paths …" (col.15 ll.20-26)
- "said cell selection means comprising an expert system including a knowledge base containing rules …" (col.15 ll.49-58)
- "said data path generator means comprising a knowledge base containing rules for selecting data paths …" (col.15 ll.59-68)
- "a knowledge base containing rules for selecting hardware cells …" (col.16 ll.21-23)
- "expert system means operable with said knowledge base for translating the flowchart …" (col.16 ll.24-29)
- "storing in an expert system knowledge base a set of rules for selecting hardware cells …" (col.16 ll.42-44)

- "applying to the specified definition of the action or condition to be performed, a set of cell selection rules stored in said expert system knowledge base" (col.16 ll.53-65)
- "applying to the selected cells a set of data path rules stored in a knowledge base ..." (col.16 ll.4-7)
- "storing in a knowledge base a set of rules for selecting hardware cells ..." (col.17 ll.19-22)
- "applying rules of said knowledge base to the specified macros to select from said cell library the hardware cells required ..." (col.18 ll.6-14)
- "storing in said knowledge base a set of rules for creating data paths between hardware cells" (col.18 ll.17-18)
- "applying rules of said knowledge base to the specified means to create data paths for the selected hardware cells" (col.18 ll.19-21)

The use of an expert system knowledge base incorporating rules for use with an inference engine for selecting cells, synthesizing data paths and synthesizing control structures, is taught in the following references:

B-i. IBM EDS
B-ii. CMU DAA
B-iii. AT&T DAA
B-iv. HAL
B-v. Fujitsu DDL/SX
B-vi. CATHEDRAL
B-vii. CHIPPE
B-viii. NTT VLSI-DE
B-ix. [Rosenstiel86b]
B-x. [Brewer86]
B-xi. [Gajski84]
B-xii. [Birmingham86]
B-xiii. [Wolf86]

The teachings in the references above to use an inference engine with a knowledgebase incorporating rules to select cells, synthesize data paths and control structures, could be combined with the synthesis systems described in the following references to render the claim obvious:

B-1. MEGA
B-2. SOCRATES
B-3. Berkeley SYNTHESIS SYSTEM
B-4. Ancestral DC
B-5. Carleton ELF
B-6. DAGON
B-7. FLAMEL
B-8. CADDY
B-9. PLEX

If the claim construction is so broad as to not require the use of an expert system inference engine, then SOCRATES taught the use of an expert system knowledge base incorporating rules as described and would render the claim invalid without combination.

The motivation to combine these references can be drawn from several sources:

- The extensive cross-citation between publications cited in this report describing these systems.
- The [Rosenstiel86b] article advocated the use of knowledge-based expert systems in synthesis systems. See, e.g., [Rosenstiel86] at 248-249, 254-255.
- The [Birmingham86] article advocated the application of knowledge-based expert systems to synthesis. See, e.g., [Birmingham86] at 533-534.
- The [Wolf86] describes knowledge base for module selection by expert system [Wolf86] at 867-869.
- Other publications cited in section 3 of Exhibit 19 on the literature describing synthesis systems taught that expert systems and rule bases were an appropriate and useful method for controlling the synthesis process, selecting cells, synthesizing datapaths and control paths. See Ex. 19, section 3.

C. Combination with References Teaching Datapath and Control Generation

Each of the following claim elements implicates the generation of data paths and/or control circuitry:

- "data path generator means" (col.15 ll.16-19)
- "a knowledge base containing rules for selecting data paths …" (col.15 ll.20-26)
- "control generator means" (col.15 ll.28-31)
- "data path generator means" (col.15 ll.59-68)
- "control generator means" (col.16 ll.1-4)
- "generating data paths for the selected integrated circuit hardware cells" (col.17 ll.8-10)
- "storing in said knowledge base a set of rules for creating data paths …" (col.18 ll.17-18)
- "applying rules of said knowledge base to the specified means to create data paths for the selected hardware cells" (col.18 ll.19-21)
- "steps of generating a controller and generating control paths …" (col.18 ll.22-24)

The use of a synthesis process to generate both data paths and control circuitry is taught in the following references:

C-i.	MEGA
C-ii.	CMU DAA
C-iii.	AT&T DAA
C-iv.	HAL
C-v.	FLAMEL
C-vi.	CATHEDRAL
C-vii.	CADDY
C-viii.	CHIPPE
C-ix.	NTT VLSI-DE
C-x.	Berkeley SYNTHESIS SYSTEM
C-xi.	Ancestral DC
C-xii.	Carleton ELF
C-xiii.	IBM EDS
C-xiv.	PLEX
C-xv.	Fujitsu
C-xvi.	MIMOLA & V-SYNTH
C-xvii.	[Thomas81]
C-xviii.	[Shiva83]
C-xix.	[Parker84]
C-xx.	[Rosenstiel86c]

The teachings in the references above to generate both data paths and control circuitry could be combined with the synthesis systems described in the following references to render the claims obvious:

C-1.	SOCRATES
C-2.	DAGON

The motivation to combine these references can be drawn from several sources:

- The extensive cross-citation between publications cited in this report describing these systems.
- The fact that the literature describing synthesis systems, described that both datapaths and control logic could be generated by the synthesis process. See Ex. 19, section 6, infra.
- The [Thomas81] article describes that designs include both control and data flow components and that the task of synthesis is to convert high level behavioral descriptions of each of these into logical or physical structures for both control and data flow circuitry. See, e.g., [Thomas81] at 1201-1203, FIGS. 1, 6.

- The [Shiva83] article describes that hardware synthesis includes synthesis of both data path and control functions. See, e.g., [Shiva83] at 76-77.

- The [Parker84] article teaches that synthesis includes elements of both data path synthesis and control synthesis. See, e.g., [Parker84] at 77-78.

- The [Rosenstiel86c] article teaches that synthesis includes components of data path synthesis and control synthesis. See, e.g., [Rosenstiel86c] at 36, 38.

D. Combination with References Teaching Simulation.

Each of the following claim elements implicates functional simulation of the design input:

- "flowchart simulator means" (col.15 ll.12-15)

The use of a functional simulator for simulating the behavior of a flowchart design input to a synthesis system is taught in the following references:

D-i. MEGA
D-ii. IBM EDS

The teachings in the references above to include simulators in a synthesis system to allow for simulation of the design input could be combined with the synthesis systems described in the following references to render the claims obvious:

D-1. SOCRATES
D-2. Berkeley SYNTHESIS SYSTEM
D-3. Ancestral DC
D-4. CMU DAA
D-5. AT&T DAA
D-6. HAL
D-7. DAGON
D-8. Fujitsu
D-9. CATHEDRAL
D-10. Carleton ELF
D-11. FLAMEL
D-12. CADDY
D-13. CHIPPE
D-14. NTT VLSI-DE
D-15. PLEX
D-16. Berkeley SYNTHESIS SYSTEM
D-17. MIMOLA & V-SYNTH

The motivation to combine these references can be drawn from several sources:

- The extensive cross-citation between articles describing these systems.

- The fact that the literature describing synthesis systems as a whole, described that simulation could be used to verify the functional characteristics of a design input. See Ex. 19, section 2a.

- Most of the references described above included functional simulators for evaluating the functional performance of the design input to the synthesis process. If graphical flowcharts were to be used as a design input to the systems, it would be obvious to provide a simulator for these inputs as well. See the passages identified corresponding to claim 5 in the charts for: CMU-DAA, HAL, DAGON, CATHEDRAL, NTT VLSI-DE.

E. Mask Generation Was Obvious At The Time of the Invention To A Person of Ordinary Skill in the Art.

Each of the following claim elements implicates the generation of mask data from the netlist output of the synthesis system:

- "mask data generator means" (col.15 ll.3-7)
- "mask data generator means" (col.16 ll.30-33)
- "generating from the netlist the mask data required …" (col.16 ll.66-68)

As the patent itself describes: "Computer-aided design systems for cell placement and routing are commercially available which will receive netlist data as input and will lay out the respective cells in the chip, generate the necessary routing, and produce mask data which can be directly used by a chip foundry in the fabrication of integrated circuits." ['432 patent, col.5 ll.40-46]

Other references also demonstrate that the production of mask data was a standardelement in the process of implementing semiconductor devices. This fact is established by [Mead80] at 92-98, [Gajski85] at 54.

DISCLOSURES UNDER PATENT L.R. 3-4

A. Patent L.R. 3-4(a)

Ricoh has failed to provide an identification of the accused instrumentality, which is "as specific as possible", as required by Patent L.R. 3-1(b). Despite Ricoh' failure to comply with Patent L.R. 3-1(b), Synopsys has produced internal engineering documents describing the design of its Design Compiler software and related products. In addition, the parties have agreed on terms under which Ricoh may review Synopsys' source code for its Design Compiler software.

B. Patent L.R. 3-4(b)

Synopsys has produced copies of the relevant prior art identified in this document and in the charts attached hereto.

Dated: April 26, 2004

Respectfully submitted,

By: _____

Christopher Kelley (SBN 166608)

Attorneys for Plaintiff SYNOPSYS, INC. and for Defendants and Counterclaimants AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORPORATION, MATROX ELECTRONIC SYSTEMS, LTD. and MATROX TECH, INC.

CERTIFICATE OF SERVICE

I am employed in the County of San Mateo, State of California. I am over the age of eighteen (18) years and not a party to the within action; my business address is 301 Ravenswood Avenue, Menlo Park, California 94025-3434.

On April 26 , 2004, at my place of business, I caused a true and correct copy of the document described as:

SYNOPSYS, INC.'S AND DEFENDANTS AEROFLEX, ET AL.'S PRELIMINARY INVALIDITY CONTENTIONS AND ACCOMPANYING DOCUMENT PRODUCTION PURSUANT TO PATENT L.R. 3-3 AND 3-4

to be served on the parties in this action addressed as follows:

VIA FEDEX

Edward A. Meilman, Esq.
Dickstein Shapiro Morin & Oshinsky, LLP
1177 Avenue of the Americas
New York, NY 10036-2714

I declare that I am employed in the office of a member of the Bar of this Court at whose direction this service was made.

I declare under penalty of perjury under the laws of the State of California and under the laws of the United States of America that the foregoing is true and correct

I declare under penalty of perjury that the foregoing is true and correct. Executed at Menlo Park, California on April 26, 2004.

Glenda Guthart

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MATROX INTERNATIONAL CORP., and
MATROX TECH, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD.,

Plaintiff,

vs.

AEROFLEX INCORPORATED, et al.,

Defendants.

SYNOPSYS, INC.,

Plaintiff,

vs.

RICOH COMPANY, LTD.,

Defendant.

Case No. C-03-4669 MJJ (EMC)
Case No. C-03-2289 MJJ (EMC)

PRELIMINARY INVALIDITY CONTENTIONS OF SYNOPSYS AND THE CUSTOMER DEFENDANTS REGARDING U.S. PATENT 5,197,016, PURSUANT TO PATENT L.R. 3-3 AND L.R. 3-4

Pursuant to Rule 3-3 of the Patent Local Rules of Practice in Civil Proceedings before the United States District Court for the Northern District of California ("Patent L.R."), Synopsys, Inc. ("Synopsys") and Defendants Aeroflex, Inc., AMI Semiconductor Inc., Aeroflex Colorado Springs, Inc., Matrox Electronic Systems, Ltd., Matrox Graphics Inc., Matrox International Corp., and Matrox Tech, Inc. (collectively "Defendants") submit the following Preliminary Invalidity Contentions ("Invalidity Contentions") regarding U.S. Patent 5,197,016 ("the '016 patent").

- Exhibits 1 and 2 provide Synopsys' and the Defendants' disclosure pursuant to Patent L.R. 3-3(c) for the '016 patent.
- The remainder of Synopsys' and the Defendants' disclosure pursuant to Patent L.R. 3-3(a), (b), (c), and their disclosure under subsection (d) for the '016 patent are contained herein.

Synopsys and Defendants base these Invalidity Contentions on their current knowledge, understanding, and belief as to the facts and information available as of the date of these contentions. Synopsys and Defendants have not yet completed their investigation, collection of information, discovery, or analysis relating to this action, and additional discovery may require them to supplement, amend and/or modify these contentions. More specifically, Ricoh has not produced all of the information responsive to Synopsys' discovery requests. Synopsys and the Defendants also have not had the opportunity to take any of the depositions of the named inventors of the '016 patent, and/or other persons having potentially relevant information. Synopsys and the Defendants also continue to search for additional invalidating prior art for the asserted claims of the '016 patent. Consequently, based upon a showing of good cause, Synopsys and the Defendants may subsequently seek an order from the Court allowing it to amend, modify, or supplement these contentions within a reasonable time after the discovery of any additional invalidating prior art.

Synopsys' and the Defendants' ultimate contentions concerning the validity of the '016 patent claims may change based upon the Court's construction of the claims and/or positions that Ricoh may take concerning claim construction, infringement, and/or validity issues.

The accompanying documents as well as the information provided below and in the Exhibits are provided for Synopsys' and the Defendants' compliance with Patent Local Rules 3-3 and 3-4 only. The information provided shall not be deemed an admission regarding the scope of any claims or the proper construction of those claims or any terms contained therein. The fact that documents have been identified below and produced with these Invalidity Contentions shall not be deemed an admission that such documents are admissible and/or that Synopsys and the Defendants have waived any objections regarding the admissibility of such documents.

DISCLOSURES UNDER PATENT L.R. 3-3(D)

I. INVALIDITY OF '016 PATENT UNDER 35 U.S.C. § 112

A. Knowledge Base Not Adequately Disclosed

The '016 patent fails to meet the "enablement" requirement of 35 U.S.C. § 112, because the '016 specification does not provide an explanation or disclosure of the expert system rules used by the described CAD system sufficient to allow one of ordinary skill in the art to build the expert system knowledge base referred to by the patent specification. The BLATH (Block Level Aaf to Hardware) software described in the specification relies on this knowledge base to perform a variety of functions critical to successful operation of the system. *See, e.g.,* '016 patent, col.2 ll.14-18, col.2 l.65 – col.3 l.8, col.5 ll.11-15, col.9 ll.59-64, col.9 l.68 – col.10 l.2.

In particular, the '016 patent fails to provide sufficient information to allow one of ordinary skill in the art to implement an expert system knowledge base capable of performing: (1) selection of macros, (2) merging two macros, (3) mapping of macros to cells, (4) merging two cell, or (5) error diagnostics. *See* '016 patent, col.10 ll.8-14. The '016 patent also fails to provide sufficient information to allow one of ordinary skill in the art to implement an expert system knowledge base capable of performing: (1) map arguments to data paths, (2) map actions to macros, (3) connect blocks, (4) remove cells, (5) reduce multiplexor trees, and (6) use fan-out. *See* '016 patent, col.10 l.23 – col.11 l.38.

In addition, the '016 patent provides no information about how BLATH might select between hardware or software cells when the functional specifications provided by the user are free of

indication that an intended function is implemented on the hardware subsystem or software subsystem. *See* '016 patent, col.5 ll.11-15.

The failure to adequately describe the knowledge base may additionally constitute a violation of the written description and/or best mode requirements of 35 U.S.C. § 112. The operation of the knowledge base is implicated in at least the claim terms "computer operated means for translating the architecture independent functional specifications" (cl.1), "means defining a microprocessor for executing the software instructions" (cl.1), "means defining hardware elements for executing the hardware functions" (cl.1), "means defining interconnections" (cl.1), "selection means for selecting" (cl.2, 4, 19), "an expert system including a knowledge base" (cl.3, 4), "design constraint rules" (cl.12), "means for generating a netlist" (cl.15), "knowledge base containing rules" (cl.20), "expert system knowledge base" (cl.21), "selecting from said hardware cell library stored in said computer system or from said software subroutine library stored in said computer system" (cl.21), "applying to the specified definition of the action or condition to be performed, a set of cell selection rules and software subroutine selection rules stored in the knowledge base" (cl.22), "generating a netlist" (cl.23), "applying rules of said knowledge base stored in said computer system to the specified macros" (cl.25), "generating software code" (cl.28), "knowledge base" (cl.30), "implementation rules for determining the optimum implementation of macro functions" (cl.32).

An operable version of the computer-aided design system described in the '016 patent must include a knowledge base and the specification of the patent does not provide sufficient information to permit one of ordinary skill to construct such a knowledge base without undue experimentation.

B. System Controller Generation Not Adequately Disclosed

The '016 patent fails to meet the "enablement" requirement of 35 U.S.C. § 112, because the '016 specification does not provide an adequate explanation of how the CONGEN module of the described computer-aided design system generates a system controller sufficient to allow one of ordinary skill in the art to build such a computer-aided design system. The '016 patent states that the system controller is generated using a "STF file from BLATH," but says nothing about the content of this file or how it is generated. *See* '016 patent, col.5 ll.19-22, col.14 ll.39-41. The generation of a system controller is an essential element of the described CAD system. *See, e.g.,* '016 patent, col.1 ll.29-35, col.2 ll.20-24, col.4 ll.4-11, col.5 ll.22-26, col.14 ll.24-36.

The failure to adequately describe the method used for system controller generation may additionally constitute a violation of the written description and/or best mode requirements of 35 U.S.C. § 112. System controller generation is implicated in at least the claim term "control generator means for generating a controller" (cl.16).

An operable version of the CAD system described in the '016 patent must include a controller generator and the specification of the patent does not provide sufficient information to permit one of ordinary skill to construct a controller generator without undue experimentation.

C. Inference Engine Not Adequately Disclosed

The '016 patent fails to meet the "enablement" requirement of 35 U.S.C. § 112, because the '016 specification does not provide an explanation of the inference engine required by the described CAD system sufficient to allow one of ordinary skill to build such an engine. The '432 specification states that the rules interpreted by the engine must include: knowledge representation in the form of a record structure, conditional expressions in the antecedent of a rule, a facility to create and destroy structure in rule action and other capabilities. *See* '432 patent, col.10 ll.56-67. The '016 patent describes that it extends the system described in the '432 patent, but provides no additional details about the inference engine. *See* '016 patent, col.2 ll.44-46, col.3 ll.5-8, col.7 ll.29-31. The patent specification does not provide any explanation of how to implement these required capabilities and

the example rules provided do not provide any guidance since they are described in high level English rather than in the form that they would actually have to take in an operable system.

In addition, the '016 patent fails to describe how contexts are used during the operation of the PSCS software. The '432 specification describes that contexts are required and that there can be context changes. *See* '432 patent, col.10 ll.13-37. The '432 and '016 specifications, however, provide no information about how context changes are made and the relationship between contexts and the particular functions that the specification states are performed by the PSCS software. As a result, the patent specification does not provide sufficient information to enable one of ordinary skill in the art to build the system described in the specification.

The failure to adequately describe the design of the inference engine may additionally constitute a violation of the written description and/or best mode requirements of 35 U.S.C. § 112. The inference engine is implicated in all of the claim terms associated with the "Knowledge Base" and the claim terms "inference engine means" (cl.2, 4, 20).

An operable version of the CAD system described in the '016 patent must include an inference engine and the specification of the patent does not provide sufficient information to permit one of ordinary skill to construct a controller generator without undue experimentation.

D. "Architecture Independent" Lacks Adequate Definition

The '016 patent fails to meet the "written description" requirement of 35 U.S.C. § 112. The phrase "architecture independent" is used in the patent specification to distinguish the claimed invention from prior art logic synthesis systems. In the file wrapper for the '016 patent the claims of the '016 patent were distinguished from systems that perform logic synthesis on register transfer level specifications – and the 4,703,435 patent to Darringer et al. in particular – on the basis of the "architecture independent" phrase in the '016 patent claims. The phrase "architecture independent" is capable of a range of meanings, some of which would include register-transfer level descriptions and the descriptions used in the Darringer patent. Neither the text of the '016 patent nor the file wrapper provide any explanation of what meaning this phrase is to have in the context of the '016

patent and claims. The term "architecture independent" appears in each independent claim, and its use invalidates each of the claims of the patent.

DISCLOSURES UNDER PATENT L.R. 3-3(a) & 3-3(b)

II. INVALIDITY OF '016 PATENT UNDER 35 U.S.C. § 102(g)

Properly construed, the claims of the '016 patent do not read on Synopsys' Design Compiler or related products. If essential limitations of the '016 patent claims are ignored, broadening the claims so as to encompass the activities of Synopsys' Design Compiler, then individuals working at General Electric and/or other research institutions, including U.C. Berkeley, who formed Optimal Solutions and then Synopsys have a superior claim to inventorship than the named inventors of the '016 patent. The individuals who conceived of and developed the architecture of early GE / Optimal Solutions / Synopsys products included: David Gregory, Aart de Geus, William Cohen, Karen Bartlett, Karl Garrison, Gary Hachtel, Tim Moore, Russell Segal, Rick Rudell, Van Morgen and William Krieger. While each of these people may be a contributor to such an invention, the actual inventors would be determined by the scope of each claim as the Court construes it. The original conception of the architecture for GE / Optimal Solutions / Synopsys products dates back to at least 1984 and 1985. The exact date of conception and identity of the individuals forming this conception will depend upon how broadly the elements from the claims of the '016 patent are understood. Furthermore, Synopsys is not claiming that the individuals identified above are the original inventors of any general architecture relevant to this case, only that these individuals have a superior claim to inventorship of such an architecture than the persons named on the '016 patent.

III. INVALIDITY OF '016 PATENT UNDER 35 U.S.C. § 102(a) & (b)

The relevance of various prior art systems will depend upon the construction of the claims. The discussion below accounts for some, but not all, possible alternative claim constructions.

A. "input means" (cl.1) / "specification input means" (cl.4) / "flowchart editor means" (cl.13, 19) / "means for receiving user input of a list defining the series of actions and conditions" (cl.14) / "macro specification means" (cl.19) / "describing ... a series of architecture independent actions and conditions" (cl.21, 25) / "specifying ... one of said stored definitions from the macro library" (cl.21, 25) / "creating a flowchart" (cl.26)

If these claim elements are interpreted to require the use of a flowchart input constructed from a sequence of nodes describing functions to be performed or conditions to be tested, then Synopsys and the Defendants are not presently aware of any prior art that anticipates the '016 patent and includes each of the other elements of the claims of the '016 patent.

If these claim elements are interpreted broadly enough to encompass systems that use Verilog and VHDL descriptions of the target design as design inputs, then most of the claims of the '016 patent are anticipated by:

- CATHEDRAL
- MIMOLA & V-SYNTH

Charts describing the application of these prior art systems to the claims of Ricoh's patent are attached to this submission.

B. "computer operated means for translating" (cl.1) / "means defining software instructions," (cl.1) / "means defining a microprocessor" (cl.1) / "means defining hardware elements" (cl.1) / "means defining interconnections" (cl.1), / "selection means [...] for selecting" (cl.2, 4, 19) / "expert system including a knowledge base" (cl.3, 4) / "means for generating a netlist" (cl.15) / "control generator means" (cl.16) / "selection means ... for generating a netlist" (cl.19) / "knowledge base containing rules" (cl.20) / "inference engine means" (cl.20) / "storing in an expert system knowledge base ... a set of rules for selecting hardware cells or software subroutines" (cl.21) / "selecting ... appropriate integrated circuit hardware cells" (cl.21) / "applying ... a set of cell selection rules and software subroutine selection rules stored in a knowledge base" (cl.22) / "applying rules of said knowledge base ... to select ... the hardware cells and software subroutines required" (cl.25)

Many of the claim passages listed above are "means-plus-function" recitations. The exceptions are: the "expert system" recitation of claims 3 and 4, the "knowledge base containing rules" recitation of claim 20, and the "storing ... a set of rules," "selecting" and "applying" steps of claims 21, 22 and 25. Whether the claims containing these "means-plus-function" elements are anticipated by prior art will depend upon what structures described in the '016 patent are identified as "corresponding structures" for implementing the recited functions.

Whether the "means-plus-function" recitations are anticipated by particular prior art references cited herein may depend upon how much of the detailed structure of the relevant modules identified in the '016 specification for performing synthesis of circuits and generation of software (e.g. BLATH 24, knowledge base 25, CONGEN 27 and SOFTCOM 70) are identified as "corresponding structures" implementing the functions specified in the "means-plus-functions" claim passages.

If the recitations cited in the heading for this section are interpreted broadly enough to encompass systems that use rules from an expert system knowledge base and an inference engine in order to select hardware cells and generate microcode as part of the synthesis process, then the claims of the '016 patent are anticipated under 102(a) or (b) by the following references:

- CATHEDRAL

If these recitations are interpreted broadly enough to encompass systems that use heuristics or algorithms for synthesis of logic circuits and generation of microcode as part of the synthesis process, the claims of the '016 patent are anticipated by the references given above, plus:

- MIMOLA & V-SYNTH

C. "software subroutine library" (cl.2, 4, 11, 19, 21, 25)

These claim recitations are not believed to reach so broadly as to encompass any synthesis system that generates microcode as part of the synthesis process. Since Ricoh may dispute this, for the purposes of these preliminary invalidity contentions we have assumed that these recitations do reach that broadly. In that event the claims containing them are anticipated under 102(a) or (b) by the following prior art synthesis systems:

- CATHEDRAL
- MIMOLA & V-SYNTH

D. Public Use or Sale

The following logic synthesis systems are believed to have been in public use more than one year prior to January 13, 1988:

i) CATHEDRAL

Cathedral was jointly developed at the University of California at Berkeley, Phillips Research Lab, Interuniversity Micro Electronics Center, and Katholieke University, the work was sponsored by the EC under ESPRIT 97 contract. Students and professors used the system and published papers regarding the system. This system was published in the Proceedings of the IEEE Int'l Symposium On Circuits and Systems, which was held in San Jose, California in May of 1986 and the Int'l Conference on Computer-Aided Design, which was held in Santa Clara, California, in November 9-12, 1987. Synopsys and Defendants will seek discovery of additional information regarding other public use, demonstration, or sale of the system.

ii) MIMOLA/ VSYNTH

MIMOLA/VSYNTH was developed at Honeywell Inc., in Bloomington, MN and the University of Kiel. Professors and students, and Honeywell used the system and published papers, thesis and manuals regarding the system. This system was published in multiple proceedings including: the 16th Design Automation Conference held in San Diego, California in June of 1979; the 21st Design Automation Conference held in Albuquerque, New Mexico in June 1984; 23rd Design Automation Conference held in Las Vegas, Nevada in 1986; the 17th Annual Microprogramming Workshop, held in October and November of 1984 in New Orleans, LA, and the Proceedings of the 20th Annual Workshop on Microprogramming held in Colorado Springs, Colorado in December of 1987. Synopsys and Defendants will seek discovery of additional information regarding other public use, demonstration, or sale of the system.

DISCLOSURES UNDER PATENT L.R. 3-3(b)

IV. INVALIDITY OF '016 PATENT UNDER 35 U.S.C. § 103

A. Combination with References Teaching Flowchart Inputs

Each of the following claim elements implicates the use of a graphical flowchart system as a vehicle for providing input to a synthesis system:

- "input means" (cl.1)
- "specification input means" (cl.4)
- "flowchart editor means" (cl.13, 19)

- "means for receiving user input of a list defining the series of actions and conditions" (cl.14)
- "macro specification means" (cl.19)
- "describing … a series of architecture independent actions and conditions" (cl. 21, 25)
- "specifying … one of said stored definitions from the macro library" (cl.21, 25)
- "creating a flowchart" (cl.26)

The use of a graphical flowchart system as a method for providing input to a synthesis system is taught in the following references:

A-i. MEGA references
A-ii. IBM EDS references
A-iii. [Darringer85]
A-iv. [Michener71]
A-v. [Orailoglu86]
A-vi. [Director81]
A-vii. [Gustafson82]
A-viii. [Case81]

The teachings in these references to use a graphical flowchart system as a method for providing input to a synthesis system could be combined with the synthesis systems described in the following references to render the claims obvious:

A-1. CATHEDRAL
A-2. MIMOLA & V-SYNTH

The motivation to combine these references can be drawn from several sources:

- The extensive cross-citation between articles describing these systems.
- The fact that the literature describing synthesis systems generally recognized that inputs to synthesis systems could take a variety of different forms, including flow graphs and flow charts. *See* Ex. 19 to '432 Preliminary Invalidity Disclosure, section 2.
- The fact that the literature describing synthesis systems described that they were built as hierarchies of modules and that data produced as output from one module could be supplied as an input to another module within the synthesis system. *See* Ex. 19, section 7. The outputs of the flowchart input modules of references could, with appropriate modification, be integrated with existing modules of systems A-1 through A-2.
- The [Darringer85] article (A-iii) advocated the use of flowcharts as design inputs for logic synthesis systems. [Darringer85] at xv, xix.
- The [Michener71] article (A-iv) advocated the use of flowcharts as a means of describing a system design. [Michener71] at 42.

- The [Orailoglu86] article (A-v) advocated the use of flow graphs as a design input to silicon compilers, and proposed that behavioral descriptions could be converted to flow graph representations, which would then be provided as input to the silicon compiler. [Orailoglu86] at 506-509.

- The [Director81] article (A-vi) that bluntly acknowledges that it is simply a design choice to provide input through a graphical flowchart or through textual input. [Director81] at 635.

- The [Case81] reference (A-vii) points out the flowchart description for synthesis is a graphic form of a RTL description, and identifies the algorithm for the flowchart translator as previously published information. [Case81] at 637, 2nd col. *See also* [Gustafson82] at 18, 2nd col. and 20, 2nd col.

B. Combination with References Teaching Use of An Expert System Knowledge Base

Each of the following claim elements is believed to implicate the use of an expert system knowledge base:

- "computer operated means for translating" (cl.1)
- "means defining software instructions," (cl.1)
- "means defining a microprocessor" (cl.1)
- "means defining hardware elements" (cl.1)
- "means defining interconnections" (cl.1)
- "selection means [...] for selecting" (cl.2, 4, 19)
- "expert system including a knowledge base" (cl.3, 4)
- "means for generating a netlist" (cl.15)
- "control generator means" (cl.16)
- "selection means ... for generating a netlist" (cl.19)
- "knowledge base containing rules" (cl.20)
- "inference engine means" (cl.20)
- "storing in an expert system knowledge base ... a set of rules for selecting hardware cells or software subroutines" (cl.21)
- "selecting ... appropriate integrated circuit hardware cells" (cl.21)
- "applying ... a set of cell selection rules and software subroutine selection rules stored in a knowledge base" (cl.22)
- "applying rules of said knowledge base ... to select ... the hardware cells and software subroutines required" (cl.25)

The use of an expert system knowledge base incorporating rules for use with an inference engine for selecting cells, synthesizing data paths and synthesizing control structures, is taught in the following references:

B-i. IBM EDS
B-ii. CMU DAA
B-iii. AT&T DAA

B-iv. HAL
B-v. Fujitsu DDL/SX
B-vi. CATHEDRAL
B-vii. CHIPPE
B-viii. NTT VLSI-DE
B-ix. [Rosenstiel86b]
B-x. [Brewer86]
B-xi. [Gajski84]
B-xii. [Birmingham86]
B-xiii. [Wolf86]

The teachings in the references above to use an inference engine with a knowledge base incorporating rules to select cells, synthesize data paths and control structures, could be combined with the synthesis systems described in the following references to render the claim obvious:

B-1. MIMOLA & V-SYNTH

The motivation to combine these references can be drawn from several sources:

- The extensive cross-citation between publications cited in this report describing these systems.
- The [Rosenstiel86b] article (B-ix) advocated the use of knowledge-based expert systems in synthesis systems. *See, e.g.,* [Rosenstiel86] at 248-249, 254-255.
- The [Birmingham86] article (B-xii) advocated the application of knowledge-based expert systems to synthesis. *See, e.g.,* [Birmingham86] at 533-534.
- The [Wolf86] article (B-xiii) describes knowledge base for module selection by expert system. *See, e.g.,* [Wolf86] at 867-869.
- Other publications cited in section 3 of Exhibit 19 to the Preliminary Invalidity Contentions for the '432 patent on the literature describing synthesis systems taught that expert systems and rule bases were an appropriate and useful method for controlling the synthesis process, selecting cells, synthesizing datapaths and control paths. *See* Ex. 19, section 3.

E. Mask Generation Was Obvious At The Time of the Invention To A Person of Ordinary Skill in the Art.

Each of the following claim elements implicates the generation of mask data from the netlist output of the synthesis system:

- "mask data generator means" (cl.17)
- "generating from said netlist the mask data required …" (cl.24)

As the patent itself describes: "From this detailed structural level definition it is possible, using either known manual techniques or existing VLSI CAD layout systems to generate the detailed chip level geometrical information (e.g. mask data) required to produce the particular application specific integrated circuit in chip form." ['016 patent, col.2 ll.28-33] The patent also states: "The netlist 15 can be used as input to any existing VLSI layout and routing tool 16 to create mask data 18 for geometrical layout." ['016 patent, col.4 ll.11-13].

Other references also demonstrate that the production of mask data was a standard element in the process of implementing semiconductor devices. This fact is established by [Mead80] at 92-98 and [Gajski85] at 54.

DISCLOSURES UNDER PATENT L.R. 3-4

A. Patent L.R. 3-4(a)

Ricoh has failed to provide an identification of the accused instrumentality, which is "as specific as possible", as required by Patent L.R. 3-1(b). Despite Ricoh' failure to comply with Patent L.R. 3-1(b), Synopsys has produced internal engineering documents describing the design of its Design Compiler software and related products. In addition, the parties have agreed on terms under which Ricoh may review Synopsys' source code for its Design Compiler software.

B. Patent L.R. 3-4(b)

Synopsys has produced copies of the relevant prior art identified in this document and in the charts attached hereto.

Dated: May 14, 2004

Respectfully submitted,

By: _____

Christopher Kelley (SBN 166608)

Attorneys for Plaintiff SYNOPSYS, INC. and for Defendants and Counterclaimants AEROFLEX INC., AEROFLEX COLORADO SPRINGS, INC., AMI SEMICONDUCTOR, MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP., MATROX ELECTRONIC SYSTEMS, LTD. and MATROX TECH, INC.

CERTIFICATE OF SERVICE

I am employed in the County of San Mateo, State of California. I am over the age of eighteen (18) years and not a party to the within action; my business address is 301 Ravenswood Avenue, Menlo Park, California 94025-3434.

On May 14, 2004, at my place of business, I caused a true and correct copy of the document described as:

PRELIMINARY INVALIDITY CONTENTIONS OF SYNOPSYS AND THE CUSTOMER DEFENDANTS REGARDING U.S. PATENT 5,197,016, PURSUANT TO PATENT L.R. 3-3 AND L.R. 3-4

to be served on the parties in this action addressed as follows:

VIA FEDEX

Edward A. Meilman, Esq.
Dickstein Shapiro Morin & Oshinsky, LLP
1177 Avenue of the Americas
New York, NY 10036-2714

I declare that I am employed in the office of a member of the Bar of this Court at whose direction this service was made.

I declare under penalty of perjury under the laws of the State of California and under the laws of the United States of America that the foregoing is true and correct

I declare under penalty of perjury that the foregoing is true and correct. Executed at Menlo Park, California on May 14, 2004.

Glenda Guthart

Teresa M. Corbin (SBN 132360)
Christopher L. Kelley (SBN 166608)
Thomas C. Mavrakakis (SBN 177927)
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Attorneys for Plaintiff Synopsys, Inc.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

SYNOPSYS, INC., Plaintiff, vs. RICOH COMPANY, LTD., a Japanese corporation., Defendant.	Case No. C03-02289 MJJ SYNOPSYS, INC.'S RESPONSES TO RICOH COMPANY, LTD.'S FIRST SET OF INTERROGATORIES

PROPOUNDING PARTY: Defendant Ricoh Company Ltd.

RESPONDING PARTY: Plaintiff Synopsys, Inc.

SET NUMBER: One (1)

Pursuant to Rule 33 of the Federal Rules of Civil Procedure, Plaintiff Synopsys, Inc. ("Synopsys") objects and responds to Defendant Ricoh Company Ltd.'s ("Ricoh") First Set of Interrogatories to Synopsys as follows:

I. GENERAL OBJECTIONS

The following general objections should be interpreted to apply to each individual interrogatory as if set forth in full in response to each individual interrogatory:

1. Synopsys objects to Ricoh's First Set of Interrogatories as well as the instructions and definitions for them to the extent that Ricoh seeks to impose an obligation greater than those imposed by the relevant Federal Rules of Civil Procedure and the Local Rules in this District.

2. Synopsys objects to Ricoh's First Set of Interrogatories as well as the instructions and definitions for them to the extent that Ricoh seeks information protected by the attorney-client privilege, the attorney work product immunity, and/or any other recognized privilege or immunity from discovery.

3. Synopsys objects to Ricoh's First Set of Interrogatories as well as the instructions and definitions for them to the extent that Ricoh seeks information not relevant to any claim or defense in this action, or that are not reasonably calculated to lead to the discovery of admissible evidence in the present action.

4. Synopsys objects to Ricoh's First Set of Interrogatories as well as the instructions and definitions for them to the extent that Ricoh seeks information that is readily available from public sources.

5. Synopsys objects to Ricoh's First Set of Interrogatories as well as the instructions and definitions for them to the extent they are vague, ambiguous, overly broad, unduly burdensome, fail to reasonable identify the information sought, and/or seek a legal conclusion or expert opinion.

6. Synopsys objects to Ricoh's First Set of Interrogatories as well as the instructions and definitions for them to the extent that they are unreasonably cumulative or duplicative or seek information that is obtainable from some other source that is more convenient, less burdensome, or less expensive.

7. Synopsys objects to Ricoh's First Set of Interrogatories as well as the instructions and definitions for them to the extent that they seek information for time periods beyond those relevant to the claims and defenses in the instant action on the grounds that such requests are overly broad, unduly burdensome, and seek information that is neither relevant nor reasonably calculated to lead to the discovery of admissible evidence in the present action.

8. Synopsys objects to Ricoh's First Set of Interrogatories as well as the instructions and definitions for them to the extent that they seek information the production of which would violate any

Protective Order entered by a court of competent jurisdiction.

9. Synopsys objects to Ricoh's First Set of Interrogatories as well as the instructions and definitions for them to the extent that they seek information that constitutes Synopsys Trade Secrets.

10. Synopsys objects to Ricoh's First Set of Interrogatories as well as the instructions and definitions for them to the extent that they seek information in a form that is inaccessible and/or cannot be accessed without constituting an undue burden or expense to Synopsys.

11. Synopsys objects to the definition of "Documents" to the extent it is inconsistent with or goes beyond the meaning set forth in Rule 34 of the Federal Rules of Civil Procedure.

12. Synopsys objects to the definition of "Synopsys" to the extent that it seeks information from individuals or entities over which Synopsys has no control or unauthorized persons purporting to act on Synopsys' behalf.

13. Synopsys objects to the definition of "Synopsys" to the extent that it purports to include consulting experts who will not called to testify at trial. Synopsys further objects to the definition to the extent that it purports to include attorneys and therefore, any requests using such definition as seeking information protected by the attorney-client privilege and/or the attorney work product immunity.

14. Synopsys objects to the definition "ASIC Design System" to the extent that the definition is vague, overly broad, unduly burdensome and not reasonably calculated to lead to the discovery of admissible evidence.

15. Synopsys objects to the definition "ASIC Method" to the extent that the definition is vague, overly broad, unduly burdensome and not reasonably calculated to lead to the discovery of admissible evidence.

RESPONSES AND OBJECTIONS TO SPECIFIC INTERROGATORIES

INTERROGATORY NO. 1:

Identify each and every product and/or process that Synopsys has made, used, offered to sell, sold, or licensed in the United States or imported into the United States since the issue date of the '432 patent.

RESPONSE TO INTERROGATORY NO. 1:

Objection—Overly Broad/Unduly Burdensome: This discovery request imposes an undue burden on Synopsys in that this request is neither narrowly tailored to elicit information relevant to the present action nor reasonably calculated to lead to the discovery of admissible evidence.

Subject to and without waiving these objections, including the foregoing general objections, Synopsys, at this time, responds as follows: Based on Ricoh's threats of patent infringement litigation to certain of Synopsys' customers and litigation brought against certain other of Synopsys' customers, the only Synopsys software product(s) at issue in the present declaratory judgment action are: Synopsys' Design Compiler® software, the HDL Compiler® and HDL Compiler® for Verilog software that is designed for use with Design Compiler®, the Design Ware Foundation Libraries® and Design Ware Libraries ("Synopsys Accused Software").

INTERROGATORY NO. 2:

Separately for each product and/or process identified in response to Interrogatory No. 1, set forth each and every reason that tends to support or otherwise relates to Synopsys' allegation in paragraph 18 of the Compliant that "Synopsys has not made, used, offered to sell, sold, within the United States, or imported into the United States, any products or processes that infringe on any valid claim of the '432 Patent, either directly, indirectly, contributorily or otherwise, and has not induced others to infringe the '432 Patent."

RESPONSE TO INTERROGATORY NO. 2:

Subject to the foregoing general objections, Synopsys, while reserving the right to supplement based on subsequent construction of the claims of the '432 patent by the Court and information learned during discovery, responds as follows: based on Synopsys' current understanding of the claims of the '432 patent, the Synopsys Accused Software does not perform any step of:

[*with respect to claim 13 (and dependent claims)*]

(1) "storing a set of definitions of architecture independent actions and conditions." The meaning of "architecture independent actions and conditions" is an issue that will likely be resolved in claim construction. In the context of the '432 patent, "actions" and "conditions" have a very specific

meaning. The Synopsys Accused Software does not have any capacity to store definitions of "actions" and "conditions" within this meaning.

(2) "storing data describing a set of available integrated circuit hardware cells for performing the actions and conditions defined in the stored set." See above re actions and conditions.

(3) "storing in an expert system knowledge base a set of rules for selecting hardware cells to perform the actions and conditions." The Synopsys Accused Software does not incorporate an expert system knowledge base. The Synopsys Accused Software does not include rules for selecting hardware cells to perform actions and conditions, particularly as those terms are used in the '432 patent.

(4) "describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions." The Synopsys Accused Software does not accept descriptions of ASICs characterized as a series of architecture independent actions and conditions, as those terms are used in the '432 patent.

(5) "specifying for each described action and condition of the series one of said stored definitions which corresponds to the desired action or condition to be performed." The Synopsys Accused Software does not accept descriptions of ASICs characterized as a series of architecture independent actions and conditions, as those terms are used in the '432 patent. Additionally, the Synopsys Accused Software does not construct a "correspondence" relationship between any element of an input description of an ASIC and any "stored definitions" of an action and condition.

(6) "selecting from said stored data … and the interconnection requirements therefore." The Synopsys Accused Software does not employ "stored definitions" or "stored data" relating to actions and conditions, as those terms are used in the '432 patent. Furthermore the Synopsys Accused Software does not employ a "correspondence" between elements from an input characterization of an ASIC and hardware cells. The Synopsys Accused Software does not employ "cell selection rules" or an "expert system knowledge base."

[*with respect to claim 18 (and dependent claims)*]

(8) "storing in a macro library a set of macros defining architecture independent actions and conditions." The meaning of "macros" is an issue that will likely be resolved in claim construction.

Synopsys Accused Software does not employ macros defining architecture independent actions and conditions, particularly in light of the meaning of "macros," and "architecture independent actions and conditions" in the '432 patent.

(9) "storing in a cell library a set of available integrated circuit hardware cells for performing the actions and conditions." The Synopsys Accused Software does not process input designs characterized in terms of actions and conditions.

(10) "storing in a knowledge base set of rules for selecting hardware cells from said cell library to perform the actions and conditions defined by the stored macros." The Synopsys Accused Software does not employ a knowledge base or rules. It does not process input designs characterized in terms of actions and conditions. It does not use stored macros that define actions and conditions.

(11) "describing for a proposed application specific integrated circuit a flowchart comprised of elements representing a series of architecture independent actions and conditions which carry out the function to be performed by the integrated circuit." The Synopsys Accused Software does not process input designs characterized in terms of a flowchart, and does not use input designs characterized as a series of "actions" and "conditions" as those terms are used in the '432 patent.

(12) "specifying for each described action and condition of said series a macro selected from the macro library which corresponds to the action or condition." The Synopsys Accused Software does not process input designs characterized as "actions" and "conditions," and does not utilize macros that correspond to specific actions and conditions.

(13) "applying rules of said knowledge base to the specified macros to select from said cell library the hardware cells required for performing the desired function of the application specific integrated circuit and generating for the selected integrated circuit hardware cells, a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit and the interconnection requirements therefore." The Synopsys Accused Software does not use macros that correspond to specific actions and conditions. The Synopsys Accused Software does not use rules from a knowledge base.

[*with respect to other claims*]

(14) The Synopsys Accused Software does not employ:

- "input specification means" equivalent to those disclosed in the '432 patent (claim 1 and dependents),
- "cell selection means" equivalent to those disclosed in the '432 patent (claim 1 and dependents),
- "netlist generator means" equivalent to those disclosed in the '432 patent (claim 1 and dependents),
- "flowchart editor means," equivalent to those disclosed in the '432 patent (claims 9 and 11 and dependents),
- "macro specification means" equivalent to those disclosed in the '432 patent (claim 9 and dependents),
- "cell selection means" equivalent to those disclosed in the '432 patent (claim 9 and dependents),
- "data path generator means" equivalent to those disclosed in the '432 patent (claim 9 and dependents),
- "expert system means" equivalent to those disclosed in the '432 patent (claim 11 and dependents),
- a macro library defining architecture independent operations corresponding to actions and conditions (claims 1 and 9 and dependents),
- a knowledge base containing rules for selecting hardware cells (claims 1, 9 and 11 and dependents)
- design inputs characterized as a series of actions and conditions (claims 1, 9 and 11 and dependents)

Also, depending on the Court's claim construction, the ordinary use of the Synopsys Accused Software may not meet one or more of the following additional requirements in the claim limitations of

the '432 patent: a cell library; a list defining the series of actions and conditions; selecting a corresponding integrated hardware cell; generating from the netlist mask data; generating a controller and generating control paths.

In addition, any claim of the '432 patent construed by the Court to encompass the Synopsys Accused Software would render such claim invalid based on: 1) Synopsys' prior invention of the Synopsys Accused Software; 2) the prior art software from which the Synopsys Accused Software evolved; 3) the prior art of record in the file history of the '432 patent; 4) the other prior art that will be set forth in Synopsys' Patent Local Rule 3-2 disclosure; and/or, 5) the failures to comply with the written description and/or enablement requirements of 35 U.S.C. § 112 that will also be set forth in Synopsys' Patent Local Rule 3-2 disclosure.

To the extent Ricoh seeks the details of Synopsys' Invalidity Contentions or Synopsys' claim construction positions with this discovery request, Synopsys' objects to providing such contentions before the time when it is required to provide them under the applicable Patent Local Rules. *See* Patent Local Rule 2-5(a) and (c).

Synopsys may supplement and/or amend its response to this discovery request as discovery proceeds. At a minimum, the following events may be an occasion for supplementation: (i) Ricoh fully complies with all of its discovery obligations in the present action; (ii) Ricoh provides its claim construction disclosures as required by the applicable Patent Local Rules; (iii) the parties submit their Joint Claim Construction and Prehearing Statement pursuant to Patent Local Rule 4-3; and/or, (iv) the Court issues its Claim Construction Ruling in the present action. Additional supplementation may occur as necessitated by the ordinary course of discovery.

INTERROGATORY NO. 3:

Separately for each product and/or process identified in response to Interrogatory No. 1, set forth each and every reason that tends to support or otherwise relates to Synopsys' allegation in paragraph 22 of the Compliant that "Synopsys has not made, used, offered to sell, sold, within the United States, or imported into the United States, any products or processes that infringe on any valid

claim of the '016 Patent, either directly, indirectly, contributorily or otherwise, and has not induced others to infringe the '016 Patent."

RESPONSE TO INTERROGATORY NO. 3:

Objection—Overly Broad/Unduly Burdensome: This discovery request imposes an undue burden on Synopsys in that this request is neither narrowly tailored to elicit information relevant to the present action nor reasonably calculated to lead to the discovery of admissible evidence.

Subject to and without waiving these objections, including the foregoing general objections, Synopsys, at this time, responds as follows: based on Synopsys' current understanding of the claims of the '016 patent, the Synopsys Accused Software does not include at least the following:

- "input means" or equivalents disclosed in the '016 patent (claim 1 and dependent claims).
- "computer operated means" or equivalents disclosed in the '016 patent (claim 1 and dependent claims).
- "means defining software instructions of the software subsystem" or equivalents disclosed in the '016 patent (claim 1 and dependent claims).
- "means defining a microprocessor for executing the software instructions of the software subsystem" or equivalents disclosed in the '016 patent (claim 1 and dependent claims).
- "means defining hardware elements for executing the hardware functions of the hardware subsystem" or equivalents disclosed in the '016 patent (claim 1 and dependent claims).
- "means defining interconnections between the microprocessor" or equivalents disclosed in the '016 patent (claim 1 and dependent claims).
- "a macro library defining a set of architecture independent operations comprised of actions and conditions" (claims 4 & 19 and dependents). The Synopsys Accused Software does not operate on input designs characterized by "actions and conditions" as those terms are used in the '016 patent. The Synopsys Accused Software also does not employ corresponding to specific actions and conditions.

- "specification input means" or equivalents disclosed in the '016 patent (claim 4 and dependents).
- "a software subroutine library" (claims 4 & 19 and dependents). The Synopsys Accused Software does not include any library of software subroutines for deployment as microcode, firmware or other software to be used in a target system.
- "selection means" or equivalents disclosed in the '016 patent (claims 4 & 19 and dependents)
- "flowchart editor means" or equivalents disclosed in the '016 patent (claim 19 and dependents)

The Synopsys Accused Software does not perform the steps of:

- "storing in a micro library in said computer system, a set of definitions of possible architecture independent actions and conditions" (claims 21 & 25 and dependents). The Synopsys Accused Software does process input designs characterized as a series of "actions" and "conditions" as those terms are used in the '016 patent and does not employ a micro library containing macros corresponding to actions and conditions.
- "storing in a hardware cell library … data describing a set of available integrated circuit hardware cells for performing the architecture independent actions and conditions." (claims 21 & 25 and dependents). The Synopsys Accused Software does not employ hardware cell libraries containing cells corresponding to actions and conditions.
- "storing in a software subroutine library … data describing a set of software subroutines for performing the architecture independent actions and conditions." (claims 21 & 25 and dependents). The Synopsys Accused Software does not employ software subroutine libraries containing software instructions to be executed by a microprocessor included in a target integrated circuit corresponding to actions and conditions in the input circuit design.
- "describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions" (claims 21 & 25 and dependents). The Synopsys

Accused Software does not process input circuit descriptions characterized as a series of "actions" and "conditions" as those terms are used in the '016 patent.

- "storing in a knowledge base … a set of rules" (claim 25 and dependents). The Synopsys Accused Software does not utilize a knowledge base or a set of rules.
- "applying rules of said knowledge base" (claim 25 and dependents). See above.

The Synopsys Accused Software also does not use a logic synthesis process in which stored macro definitions are selected based on their correspondence to actions or conditions (claims 25 & 29) and does not implement logic identified in a design input as a microprocessor and associated software, as required by all of the claims of the '016 patent.

In addition, any claim of the '016 patent construed by the Court to encompass the Synopsys Accused Software would render such claim invalid based on: 1) Synopsys' prior invention of the Synopsys Accused Software; 2) the prior art software from which the Synopsys Accused Software evolved; 3) the prior art of record in the file history of the '016 patent; 4) the other prior art that will be set forth in Synopsys' Patent Local Rule 3-2 disclosure; and/or, 5) the failures to comply with the written description and/or enablement requirements of 35 U.S.C. § 112 that will also be set forth in Synopsys' Patent Local Rule 3-2 disclosure.

To the extent Ricoh seeks the details of Synopsys' Invalidity Contentions or Synopsys' claim construction positions with this discovery request, Synopsys objects to providing such contentions before the time when it is required to provide them under the applicable Patent Local Rules. *See* Patent Local Rule 2-5(a) and (c).

Synopsys may supplement and/or amend its response to this discovery request as discovery proceeds. At a minimum, the following events may be an occasion for supplementation: (i) Ricoh fully complies with all of its discovery obligations in the present action; (ii) Ricoh provides its claim construction disclosures as required by the applicable Patent Local Rules; (iii) the parties submit their Joint Claim Construction and Prehearing Statement pursuant to Patent Local Rule 4-3; and/or, (iv) the Court issues its Claim Construction Ruling in the present action. Additional supplementation may occur as necessitated by the ordinary course of discovery.

INTERROGATORY NO. 4:

Describe the history of the development of each and every product and/or process identified in response to Interrogatory No. 1.

RESPONSE TO INTERROGATORY NO. 4:

Objection—Overly Broad/Unduly Burdensome: This discovery request imposes an undue burden on Synopsys in that this request is neither narrowly tailored to elicit information relevant to the present action nor reasonably calculated to lead to the discovery of admissible evidence.

Objection—Vague and Ambiguous: This discovery request is rendered vague and/or ambiguous by its use of the phrase "describe the history of the development."

Subject to and without waiving these objections, including the foregoing general objections, Synopsys, at this time, responds as follows:

The Synopsys Accused Software was developed based on and/or evolved from the first releases of Synopsys' Design Compiler product, which was commercially introduced into the market as early as June 1988. The Design Compiler software was designed in 1986 and 1987 and the code for this software was written in 1987 and 1988. The Design Compiler software evolved from and included elements of the rule-based Socrates logic synthesis system developed by the founders of Synopsys when they were at General Electric's Calma division, and an algorithmic optimizer based on the MIS system developed by Rick Rudell at UC Berkeley. Mr. Rudell's work was described in his Ph.D. Qualifying Exam paper of Sept. 29, 1987. During the early 1990s the rule-based elements of the Design Compiler system were removed in favor of algorithmic-based optimization software known as "sot." The HDL compilation elements of the original Design Compiler software trace their origin to BDSyn software developed at the University of California by Russ Segal. The BDSyn software is described in Mr. Segal's Masters Thesis, dated May 2, 1987. The BDSyn software was extended to include support for verilog by the Synopsys team in early 1988.

Synopsys has continued to make improvements to the Design Compiler software and to HDL compiler software for processing HDL inputs to Design Compiler from the time of original development of these products through to the current day. It is not reasonable to attempt to describe every event in the development of these products in response to this interrogatory. If Ricoh is

interested in particular aspects of the Design Compiler software or particular design alterations, it should propound discovery directed to those specific issues.

INTERROGATORY NO. 5:

Set forth all facts and identify all documents relating to Synopsys' allegations in paragraph 29 of the complaint, including without limitation for each such fact the identity of each individual having any relevant information.

RESPONSE TO INTERROGATORY NO. 5:

Subject to the foregoing general objections, Synopsys, at this time, responds as follows:

Synopsys' claim in paragraph 29 of its Complaint for Declaratory Judgment dated May 15, 2003 that Ricoh is barred from recovery for any alleged patent infringement under the equitable principle of estoppel is based on the following facts:

1) The '432 patent issued on May 1, 1990. *See* U.S. Patent No. 4,922,432.

2) Agents of the inventors and assignees made attempts to license the '432 patent to Synopsys in 1991 and 1992. *See* Deposition of James Davis at 112:1-11; Documents Bates No. SP00154.

3) These efforts to license the '423 patent were abandoned. *See* Deposition of James Davis at 112:14-19.

4) Ricoh filed its patent infringement complaint against Aeroflex, Inc., AMI Semiconductor, Matrox Electronic Systems Ltd., Matrox Graphics Inc., Matrox Int'l, Inc., and Matrox Tech., Inc. in January 2003.

Synopsys reserves the right to supplement this interrogatory answer in light of additional information developed during discovery in this case.

Dated: December 22, 2003

Respectfully submitted,

HOWREY SIMON ARNOLD & WHITE, LLP

By: Erik K Moller /cgy
Erik K. Moller
Attorneys for Plaintiff SYNOPSYS, INC.

CERTIFICATE OF SERVICE

I am employed in the City and County of San Mateo, State of California in the office of a member of the bar of this court at whose direction the following service was made. I am over 18 years of age and am not a party to this action. My business address is 301 Ravenswood Avenue, Menlo Park, CA 94025.

On December 22, 2003, a true copy of

SYNOPSYS, INC.'S RESPONSES TO RICOH COMPANY, LTD.'S FIRST SET OF INTERROGATORIES

was served on the following:

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☒ (BY U.S. MAIL – CCP § 1013a(1)) I am personally and readily familiar with the business practice of Howrey Simon Arnold & White, LLP for collection and processing of correspondence for mailing with the United States Postal Service, and I caused such envelope(s) with postage thereon fully prepaid to be placed in the United States Postal Service at Menlo Park, California.

☒ (BY FACSIMILE – CCP § 1013(e)) I am personally and readily familiar with the business practice of Howrey Simon Arnold & White, LLP for collection and processing of document(s) to be transmitted by facsimile and I caused such document(s) on this date to be transmitted by facsimile to the offices of addressee(s) at the numbers listed below.

☐ (PERSONAL SERVICE) I caused each such envelope to be delivered by hand to the offices of each party at the address listed above.

I declare under penalty of perjury under the laws of the State of California that the above is true and correct.

Executed on December 22, 2003, at Menlo Park, CA.

Glenda L. Guthart